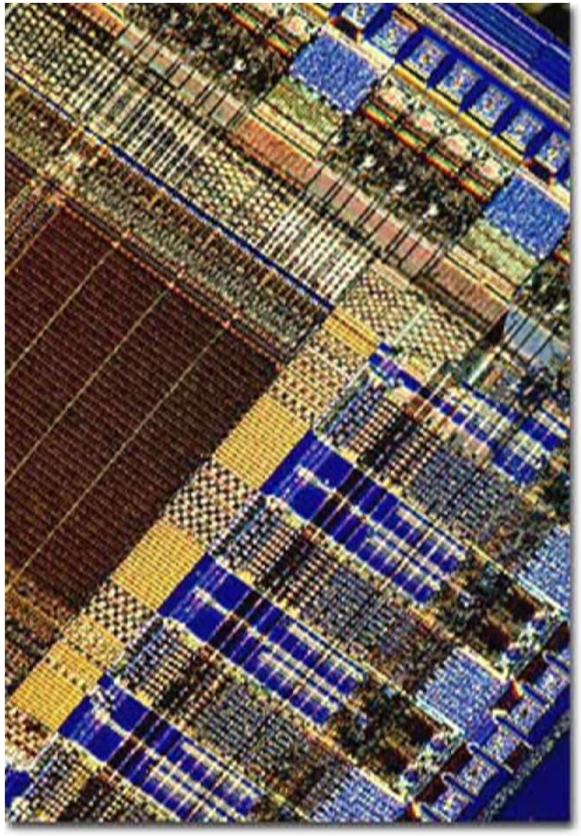
The McGraw-Hill Companies

CMOS Digital Integrated Circuits



Chapter 13
Chip Input and Output (I/O) Circuits

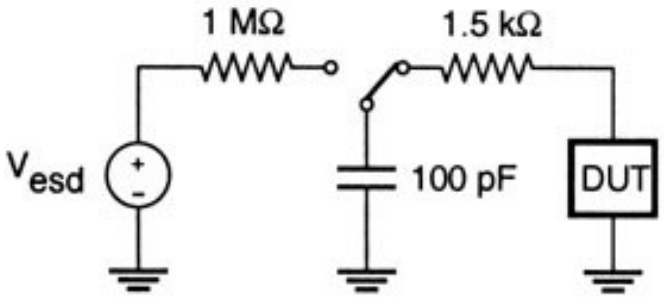
S.M. Kang, Y. Leblebici, and C. Kim

1. Scope & coverage [ ] 1-5
2. Presentation
   clarity [ ]
   chievement [ ]
3. written find report [prof]

Introduction

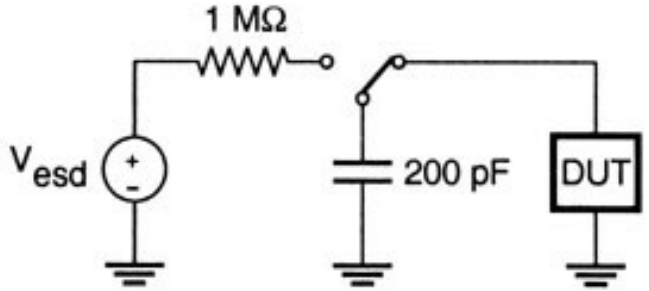
- Critical factors of reliability, signal integrity, and inter-chip communication speed
  - Clock generation and distribution
    - External clock source -> on-chip internal clock generation
  - ESD protection
    - Protection for internal circuits from external hazards
  - I/O circuits
    - CMOS <-> TTL or ECL
  - On-chip noise prevention
    - From parasitic inductance in bonding wires
  - Latch-up prevention
    - From parasitic bipolar transistors

ESD Protection



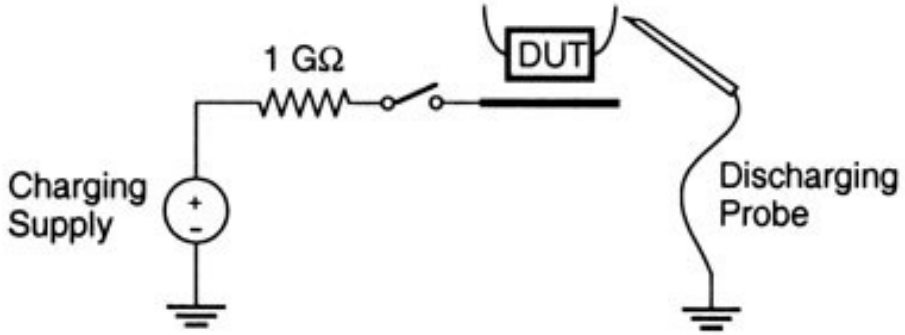
(a)

Human body model



(b)

Machine model



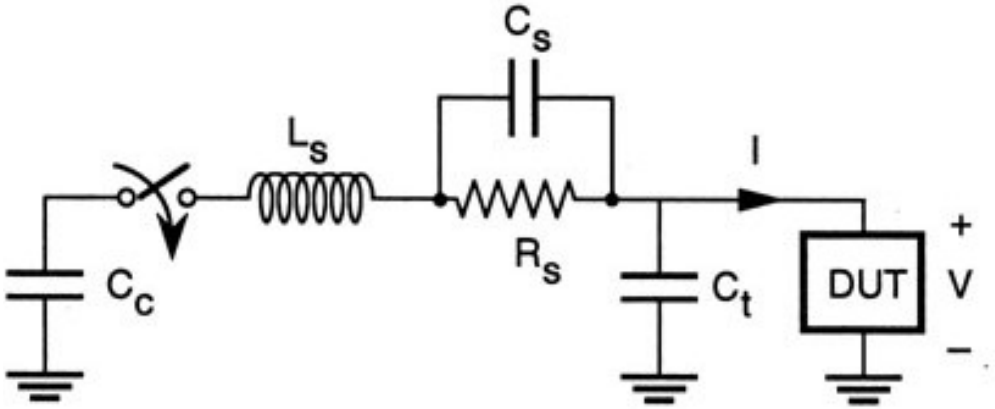
(c)

Charged device model, for ESD testing

Types of ESDs

- HBM(Human Body Model)
  - Human body can induce 1.5kV
    - Condition
      - 80% relative humidity
      - Walking on synthetic carpet
- MM(Machine Model)
  - Higher current than HBM
- CDM(Charged Device Model)
  - Discharge of the packaged IC
    - Chip assembly or shipping -> Charge accumulation -> Discharge

Simplified Lumped-Element Model of HBM-ESD and MM-ESD Testers

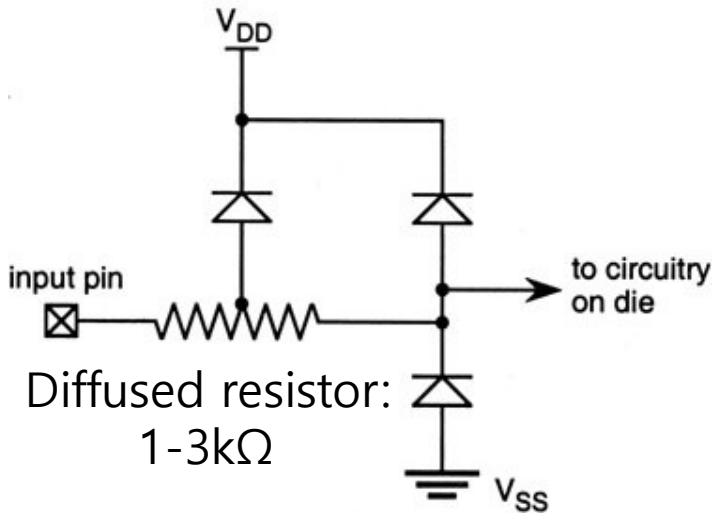


(a)

Component	HBM	MM
C_c (pF)	100	200
R_s (Ω)	1500	25
L_s (μH)	5	2.5
C_s (pF)	1	0
C_t (pF)	10	10

(b)

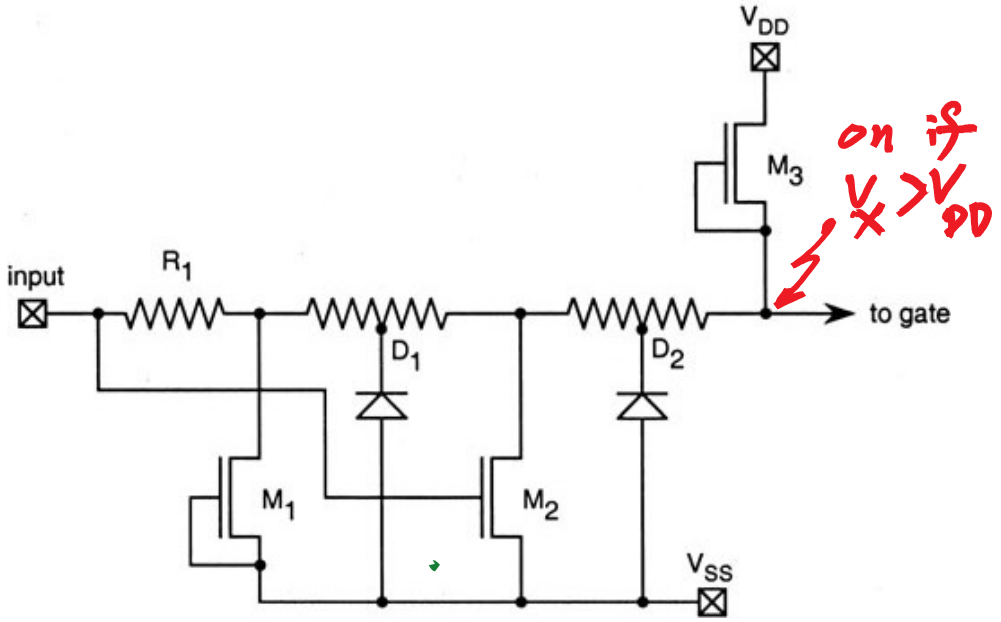
ESD Protection Network Examples



Basic ESD protection network: diodes clamp the signal level

$-0.7V < V_A < V_{DD}+0.7V$

I_D < several tens of mA

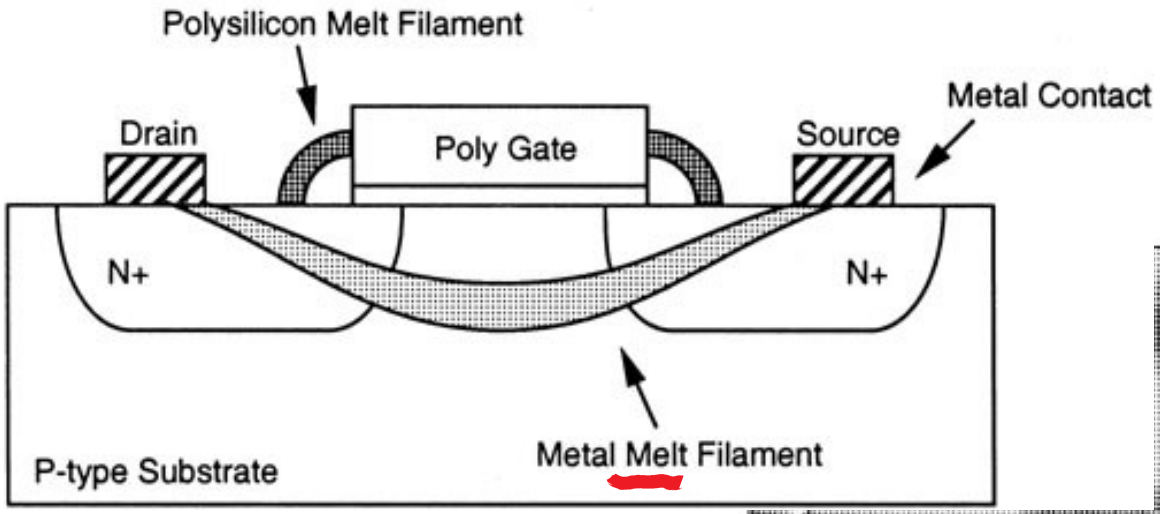


Protection network with thick-oxide transistor: effective in excess of 3kV in HBM-ESD test

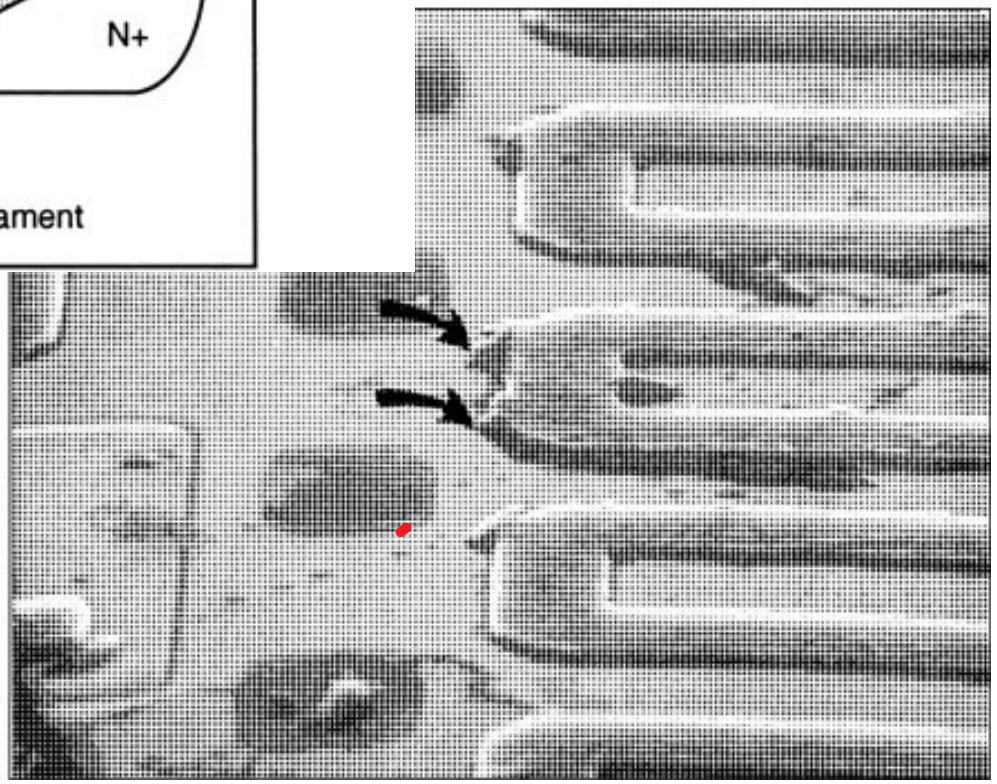
M_1, M_2: thick oxide device w/ V_T of 20~30V

M_3: thin oxide device operating in SAT region

ESD Failure

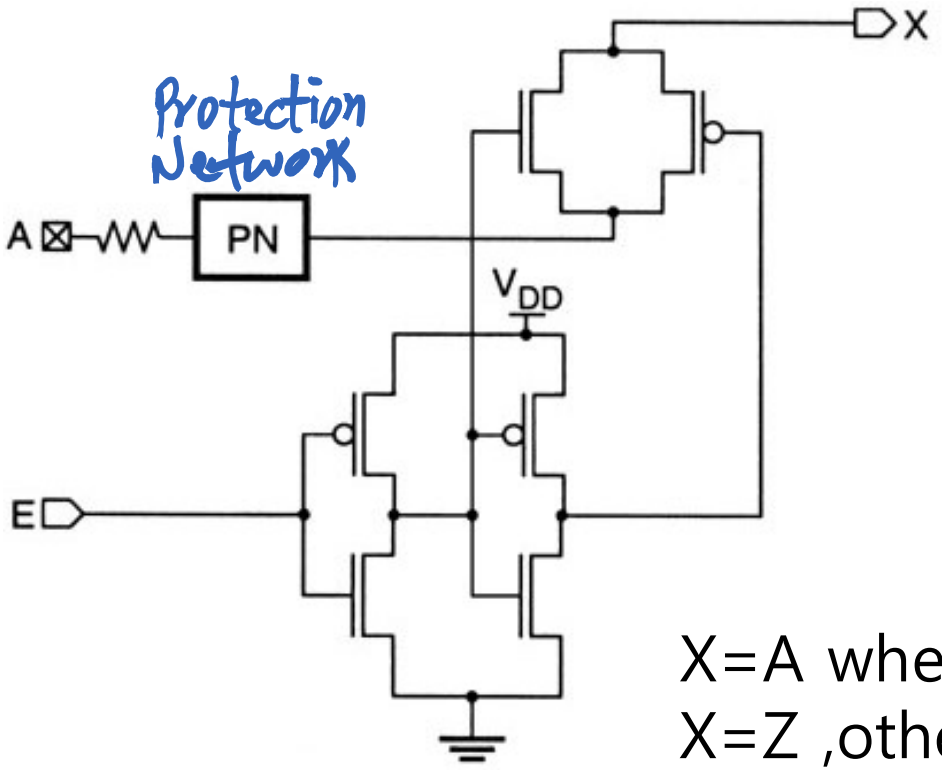


(a) Typical ESD failure modes



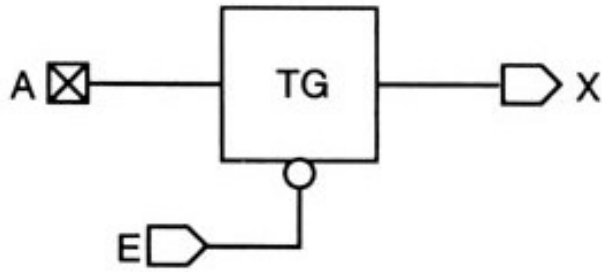
(b) SEM photograph of a failed NMOS (from Diaz *et al.*, 1994)

Input Series Transmission Gate



(a)

Schematic

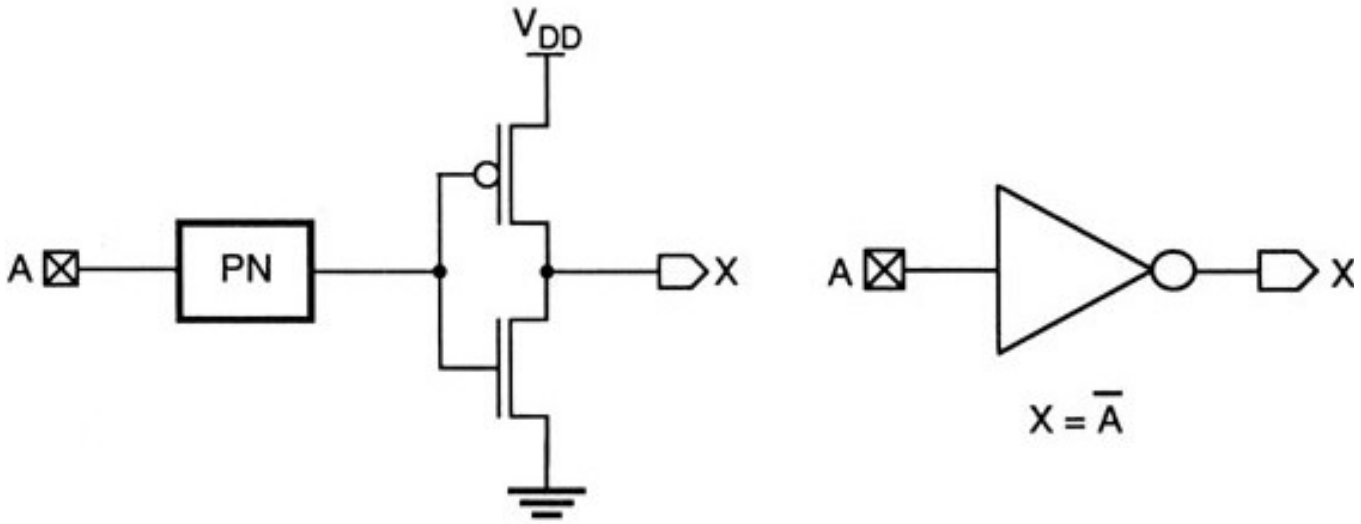


(b)

Symbol

X=A when E=0
X=Z ,otherwise

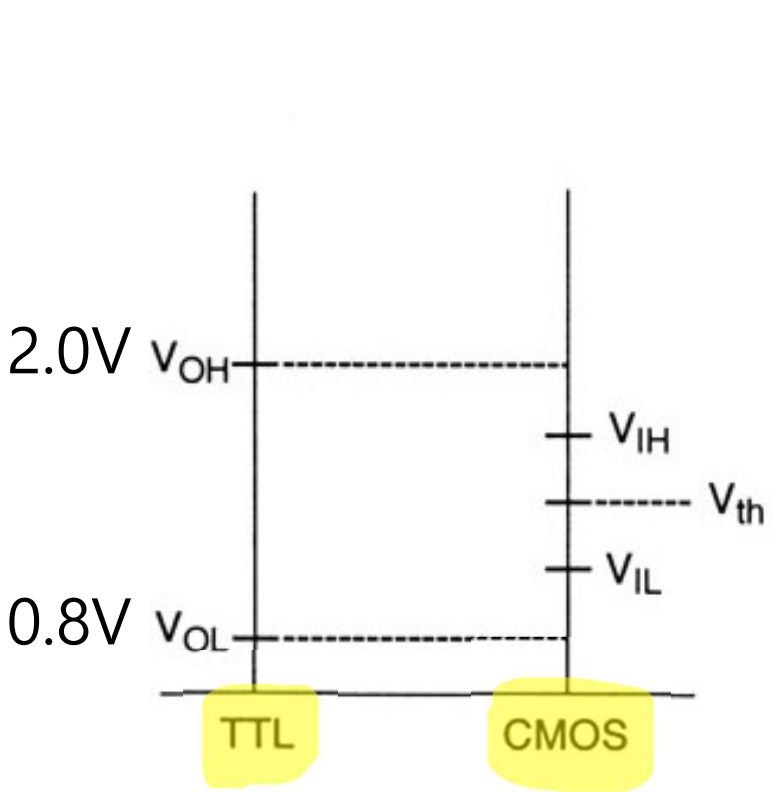
Inverting Input Circuit with PN



Schematic Symbol

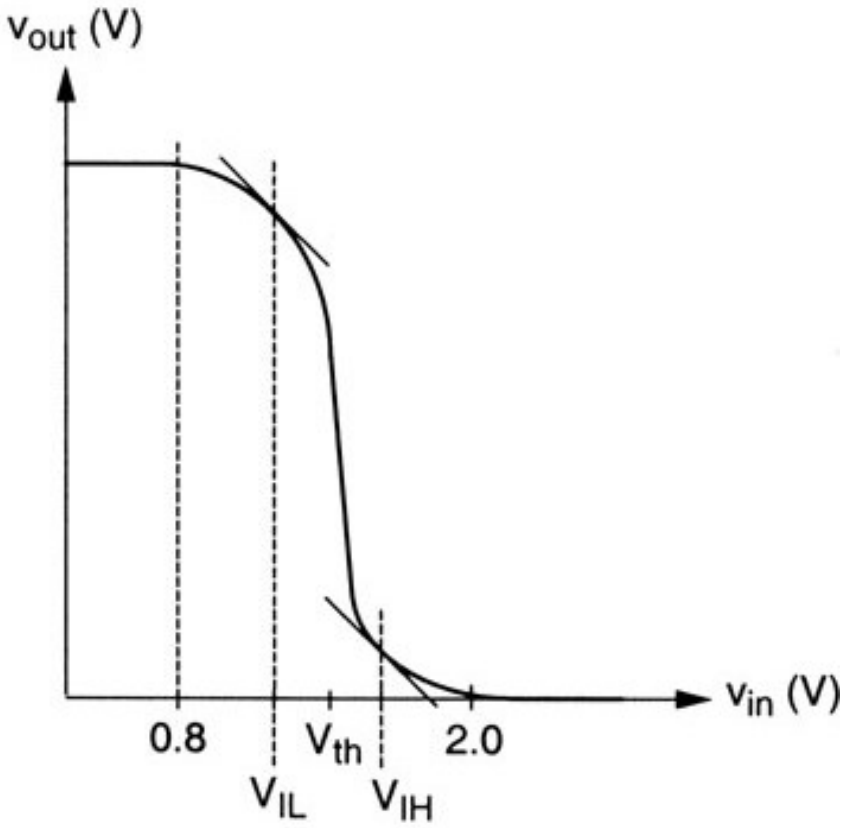
- typical $V_{IL}=0.3V_{DD}$, $V_{IH}=0.7V_{DD}$ for 30% noise margin

TTL to CMOS level shifting



(a)

Voltage level of TTL and CMOS



(b)

The corresponding VTC

Designing the Receiving Inverter Gate(1)

- Adjust the TR ratio such that the saturation voltage at which both transistors operate in saturation region is the midpoint between 0.8V and 2.0V

- Saturation voltage of the inverter gate is

$$V_{sat} = V_{th} = \frac{V_{DD} + V_{Tp} + rV_{Tn}}{1 + r}$$

$$r = \sqrt{\frac{\mu_n C_{ox} W_n / L_n}{\mu_p C_{ox} W_p / L_p}}$$

Designing the Receiving Inverter Gate(2)

- From these two equations, we get

$$\frac{W_n / L_n}{W_p / L_p} = \frac{\mu_p}{\mu_n}\left[\frac{V_{DD} + V_{Tp} - V_{sat}}{V_{sat} - V_{Tn}}\right]^2$$

- If $\mu_n = 3\mu_p$ and $V_{Tn} = -V_{Tp} = 1.0V$ and $V_{DD} = 5V$, then in order to achieve

$$V_{sat} = \frac{0.8 + 2.0}{2} = 1.4V$$

- The nMOS-to-pMOS ratio is

$$\frac{W_n / L_n}{W_p / L_p} = \frac{1}{3}\left[\frac{5 - 1 - 1.4}{1.4 - 1}\right]^2 = \frac{169}{12}$$

Designing the Receiving Inverter Gate(3)

- From the above, we get that r=6.5 and

$$V_{IL} = \frac{2V_{out} - V_{DD} + r^2 V_{Tn} + V_{Tp}}{r^2 + 1} = \frac{2V_{out} + 36.25}{43.25}$$

- where V_{out} satisfies the following:

$$\frac{r^2}{2}(V_{IL} - V_{Tn})^2 = (V_{DD} - V_{IL} + V_{Tp})(V_{DD} - V_{out}) - \frac{1}{2}(V_{DD} - V_{out})^2$$

- or

$$21.125(V_{IL} - 1)^2 = (4 - V_{IL})(5 - V_{out}) - \frac{1}{2}(5 - V_{out})^2$$

Designing the Receiving Inverter Gate(4)

- Combining these two equations,

$$21.125\left[\frac{2V_{out}-7}{43.25}\right]^2=\left[\frac{136.75-2V_{out}}{43.25}\right](5-V_{out})-\frac{1}{2}(5-V_{out})^2$$

$$V_{out}=4.97V$$

- and, hence

$$V_{IL}=\frac{2\times 4.97+36.25}{43.25}=1.07V$$

- Likewise,

$$V_{IH}=\frac{r^2(2V_{out}+V_{Tn})+V_{DD}+V_{Tp}}{r^2+1}=\frac{84.5V_{out}+47.25}{43.25}$$

Designing the Receiving Inverter Gate(5)

- where V_{out} satisfies the following

$$\frac{1}{2}(V_{DD}-V_{IH}+V_{Tp})^2 = r^2\left[(V_{IH}-V_{Tn})V_{out}-\frac{1}{2}V_{out}^2\right]$$

- or

$$\frac{1}{2}(4-V_{IH})^2 = 6.5^2\left[(V_{IH}-1)V_{out}-\frac{1}{2}V_{out}^2\right]$$

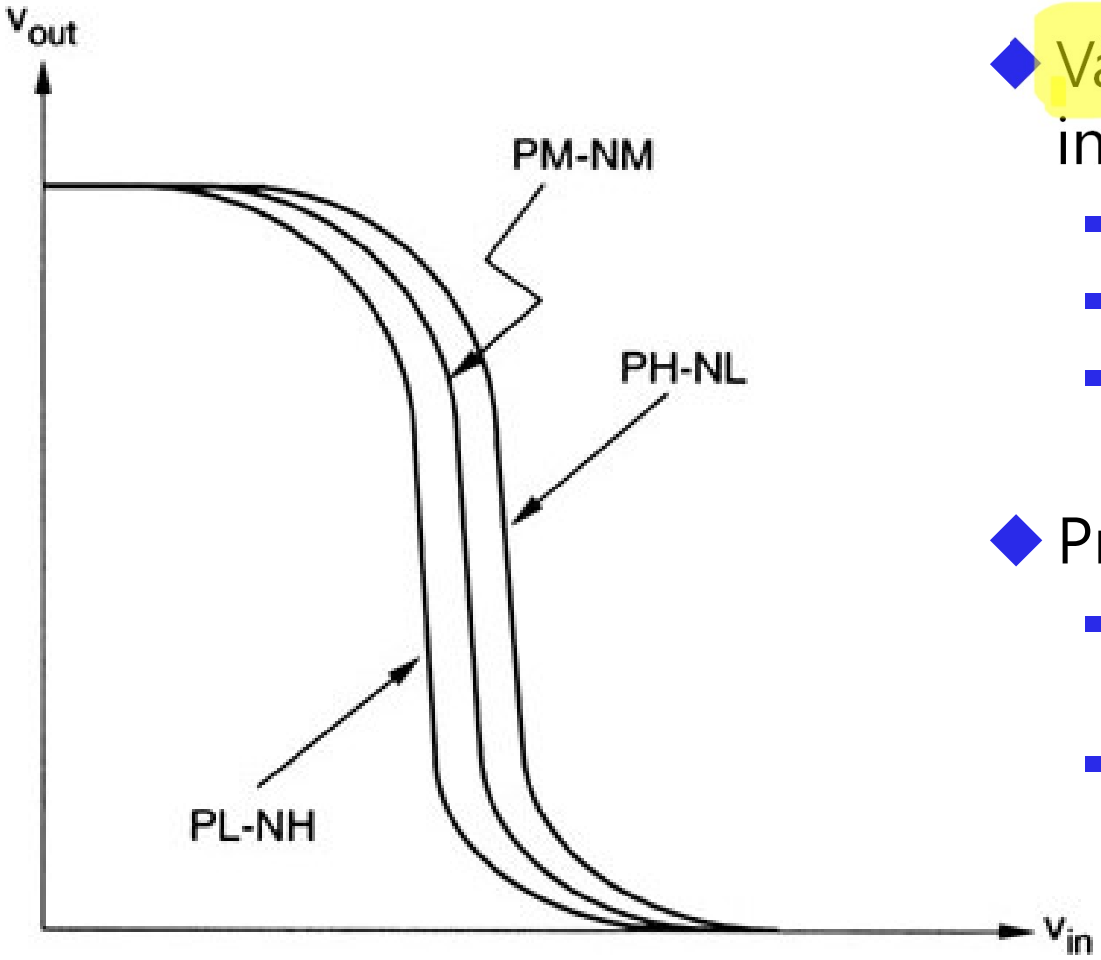
- Combining these two equations, we obtain

$$\frac{1}{2}\left(4-\frac{84.5V_{out}+47.25}{43.25}\right)^2 = 42.25\left[\left(\frac{84.5V_{out}+4}{43.25}\right)V_{out}-\frac{1}{2}V_{out}^2\right]$$

- Therefore,

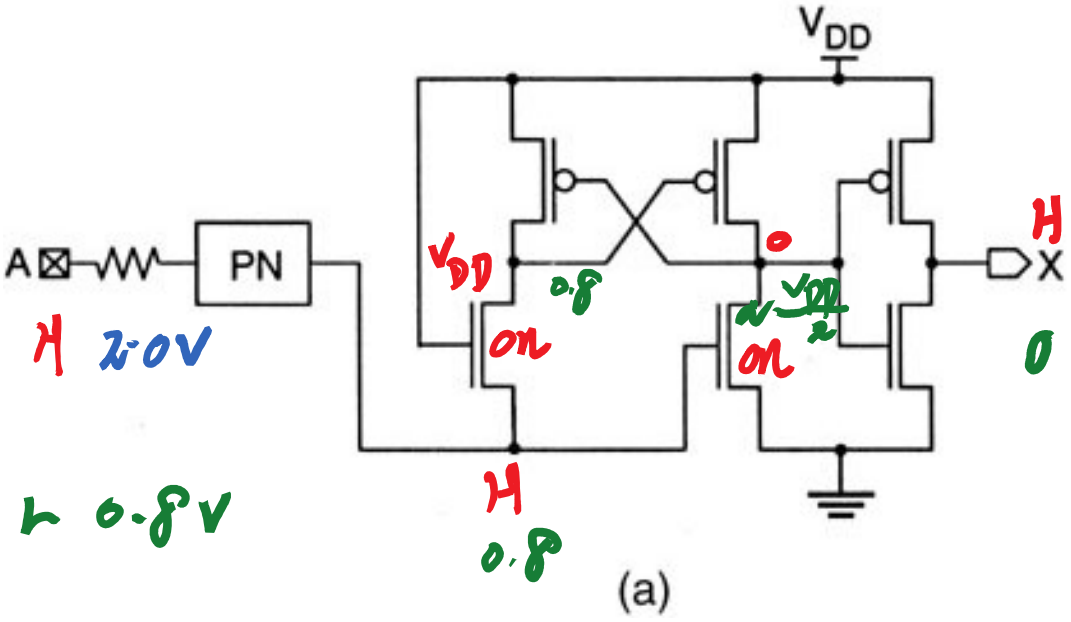
$$V_{out} = 0.206V \quad \text{and} \quad \boxed{V_{IH} = 1.47V}$$

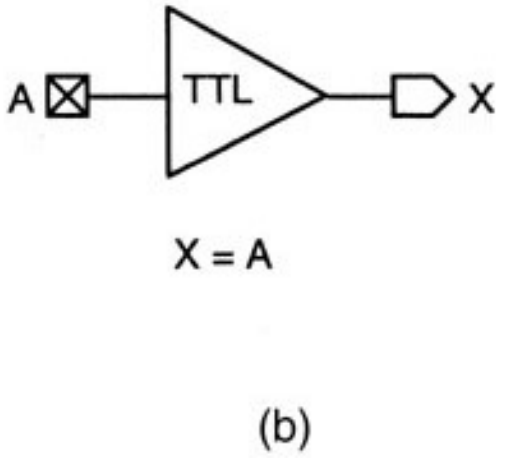
Variation of the level-shifter VTC



- Variations to consider in simulation
  - Process
  - Temperature
  - Supply voltage
- Process variation
  - Strong pMOS(PH) - Weak nMOS(NL)
  - Weak pMOS(PL) - Strong nMOS(NH)

Non-inverting TTL Level-shifting Circuit

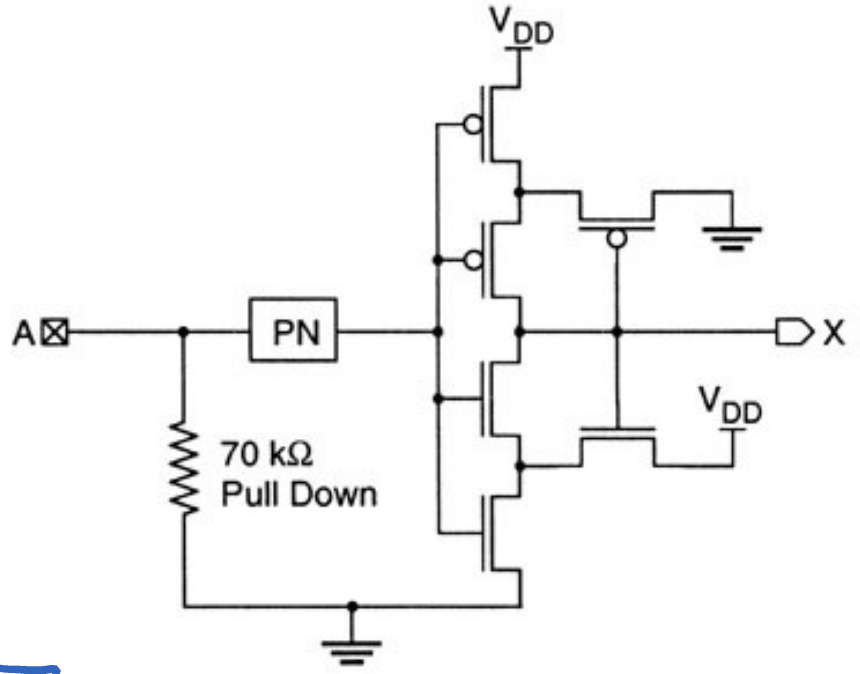




Schematic

Symbol

Input Pad Circuit with Schmitt Trigger

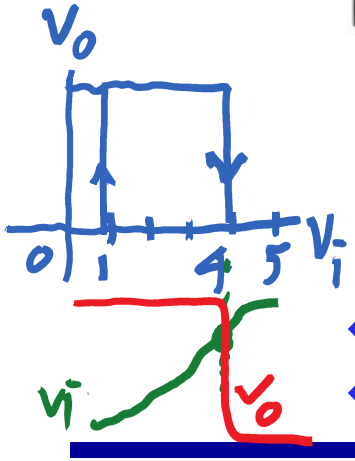


(a)

Schematic

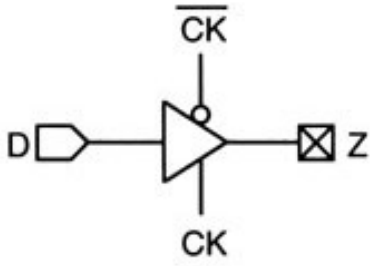
(b)

Symbol

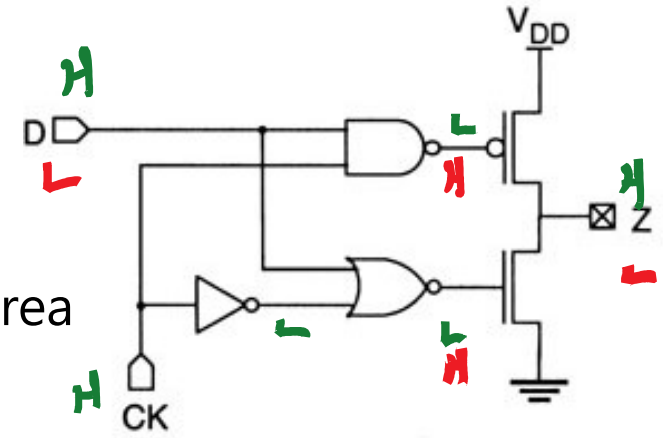


- Negative-going logic threshold voltage=1V
- Positive-going logic threshold voltage=4V

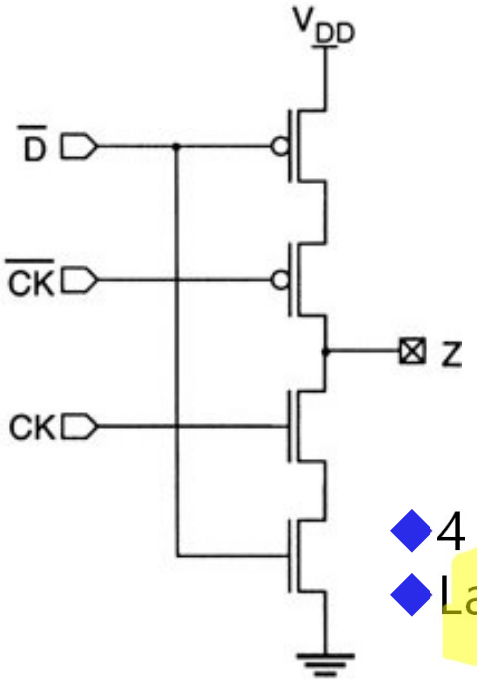
Tristable Output Circuit



(a) Symbol



(b) Circuit 1



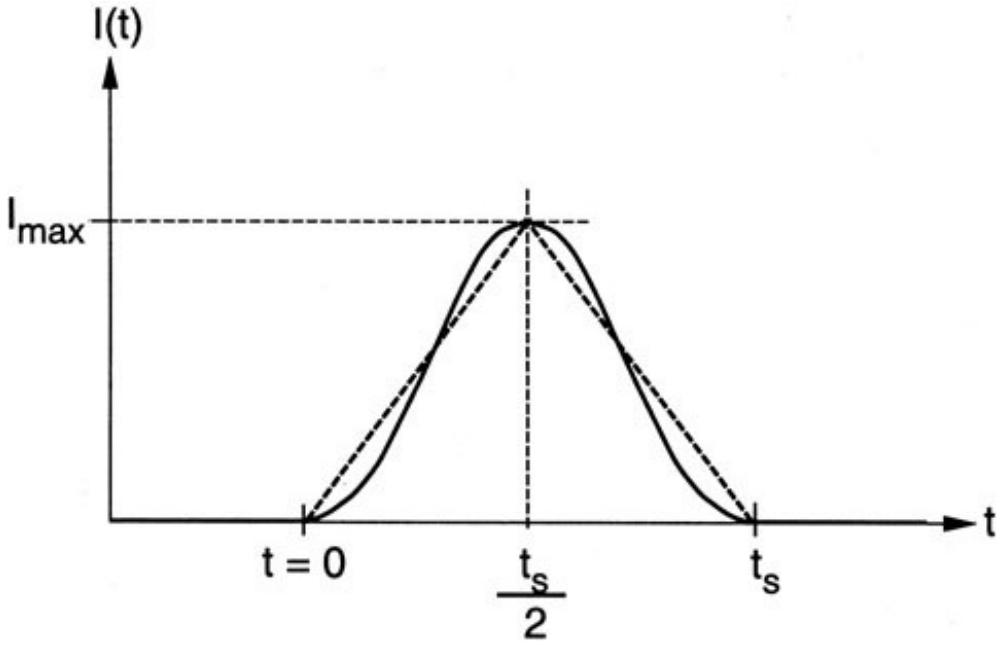
(c) Circuit 2

- 12 TRs
- Small area

- 4 TRs
- Large area

(Last stage TRs need to be large)

Typical Output Circuit Current During Switching (1)



- Capacitor load
  - Initially charged to VDD=5V
  - Sink the current to GND @ Clock signal

$$I_{max}\frac{t_s}{2} = C_{load}V_{DD}$$

$$\left[\frac{di}{dt}\right]_{max} \geq \frac{I_{max}}{t_s/2} = \frac{2I_{max}}{t_s}$$

- Thus,

$$\left[\frac{di}{dt}\right]_{max} \geq \frac{4C_{load}V_{DD}}{t_s^2}$$

Typical Output Circuit Current During Switching (2)

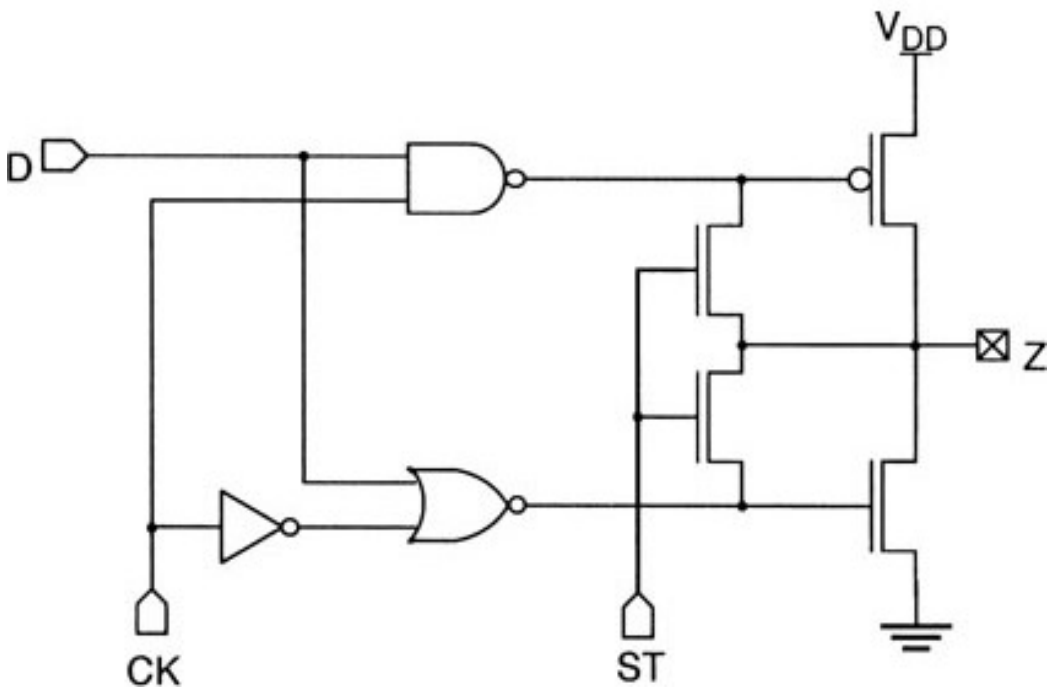
- If $C_{load} = 100\text{pF}$ and $t_s = 5\text{ns}$,

$$\left[\frac{di}{dt}\right]_{\max} \geq \frac{4 \times 100 \times 10^{-12} \times 5}{(5 \times 10^{-9})^2} = 80\,\frac{\text{mA}}{\text{ns}}$$

- And for a bonding wire with L=2,

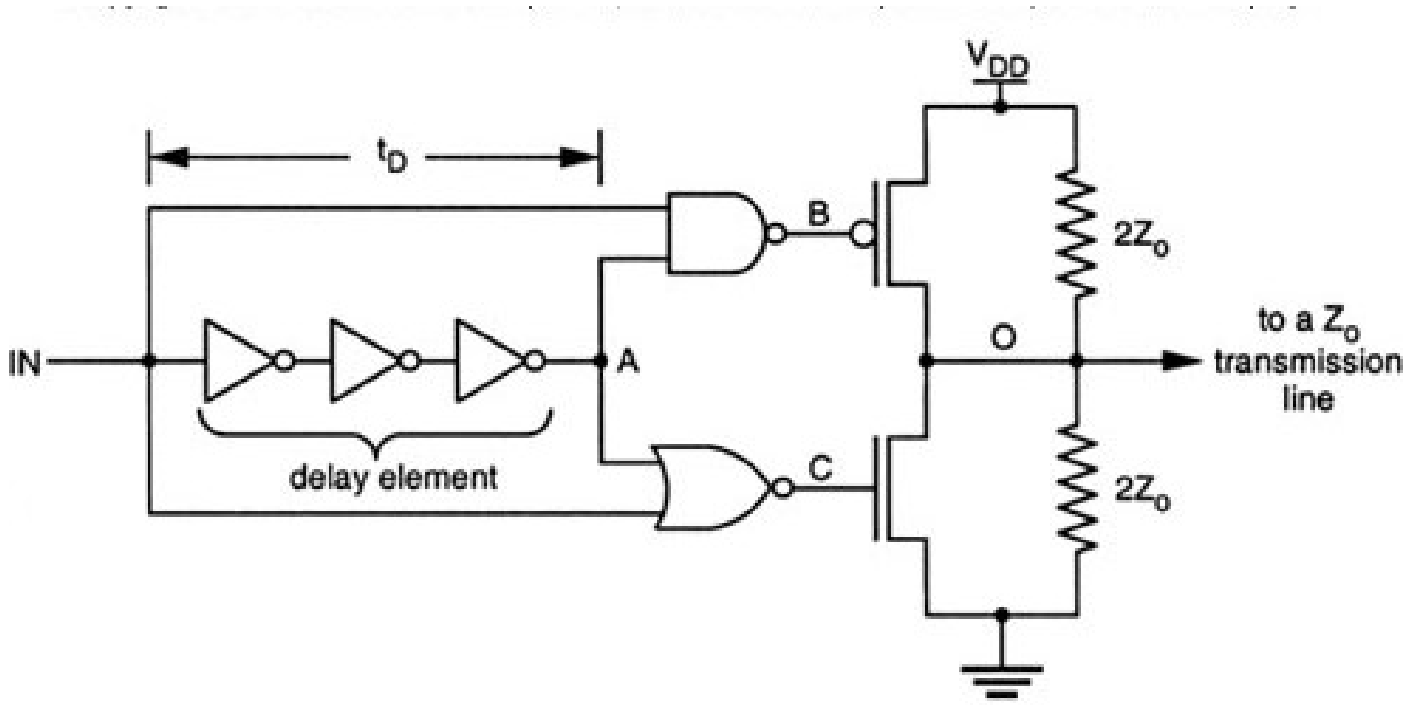
$$L\left[\frac{di}{dt}\right]_{\max} \geq 160\text{mV}$$

Circuit for Reducing (*di/dt*) Noise



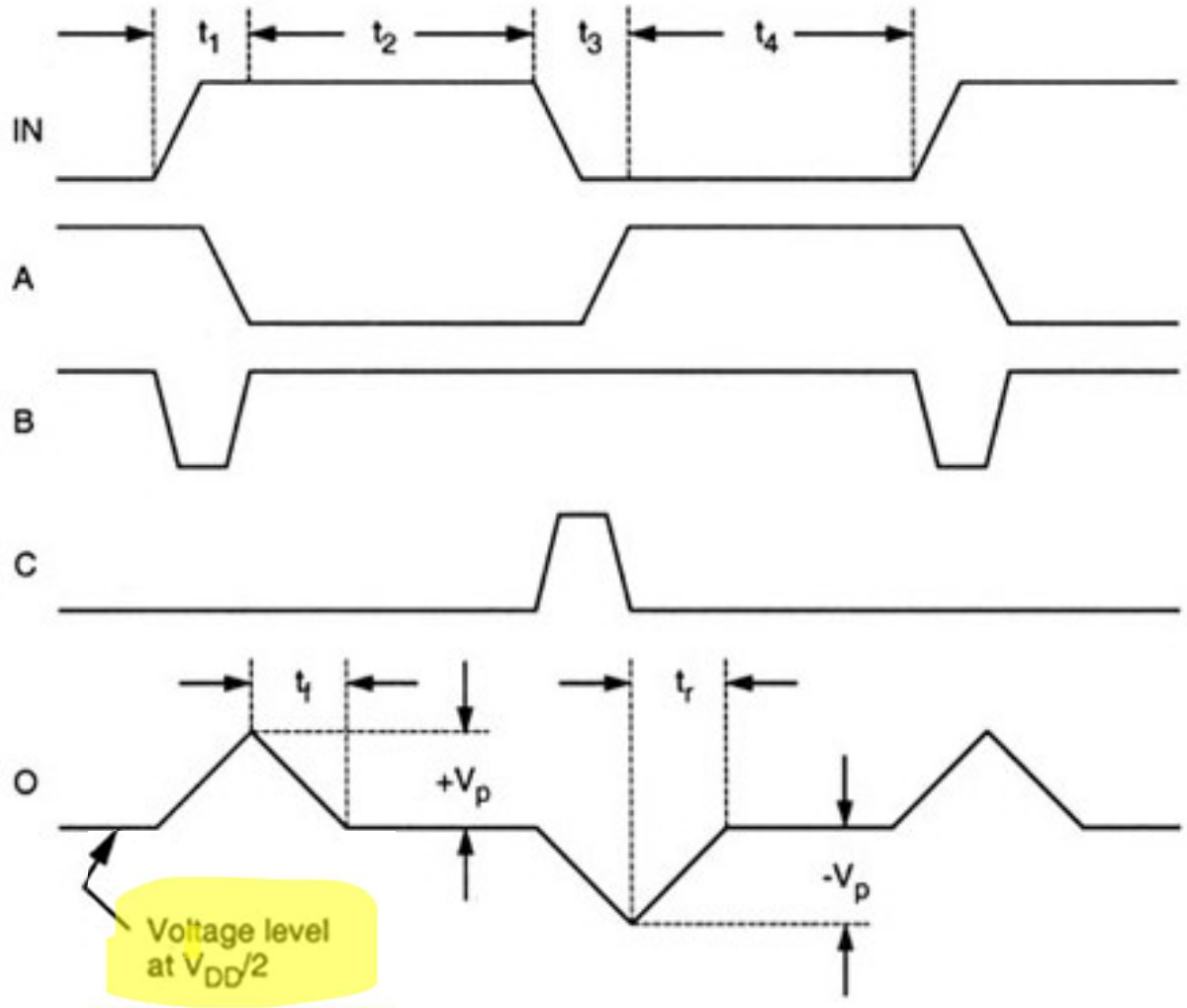
- At strobe signal(ST), the last driver TRs are precharged
- If r=1 and ST=high, the gate voltages can be precharged to VDD/2 before CK goes to high

Another Circuit for Reducing (*di/dt*) Noise



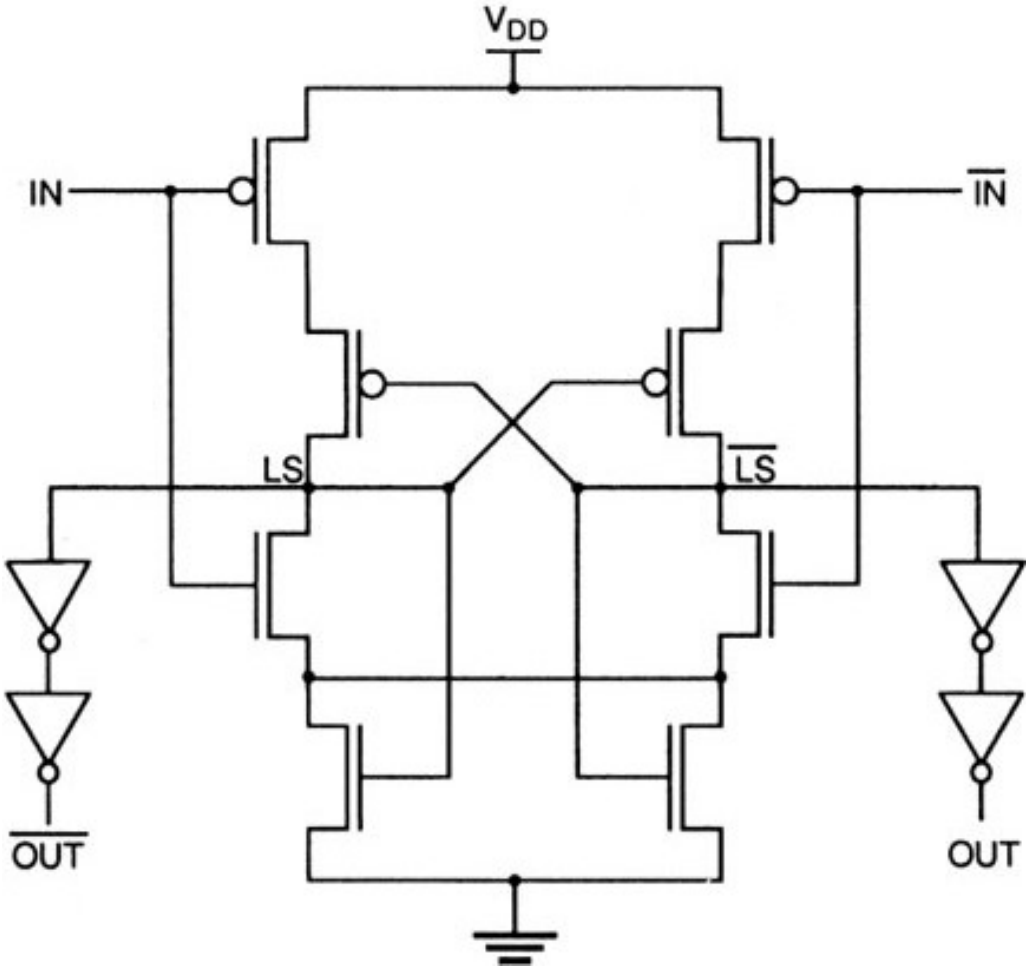
- Transmits only differential signals

Timing Diagram Of the Driver Circuit

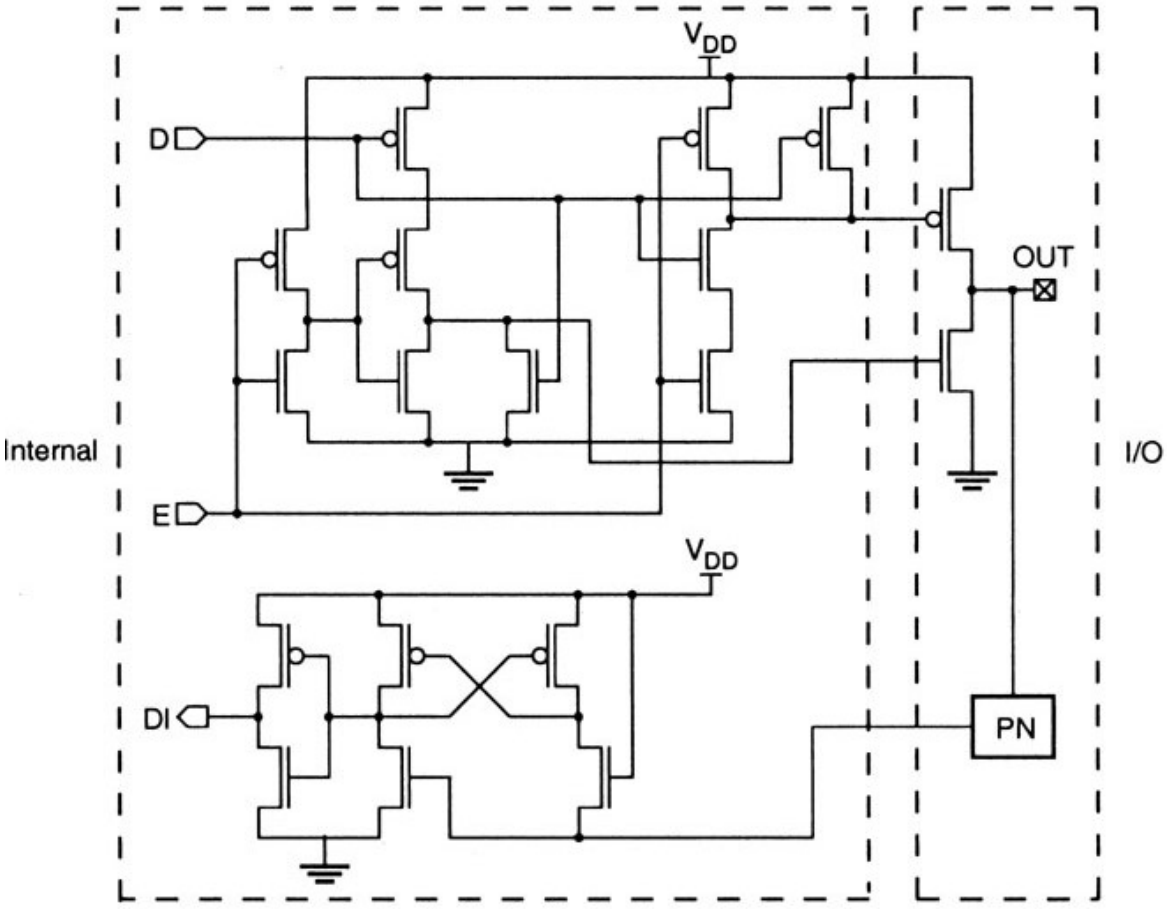


- The circuit produces pulses at nodes B and C only when input changes
- Output is at $V_{DD}/2$ during the quiescent periods
- Phase splitter is used to generate differential pairs

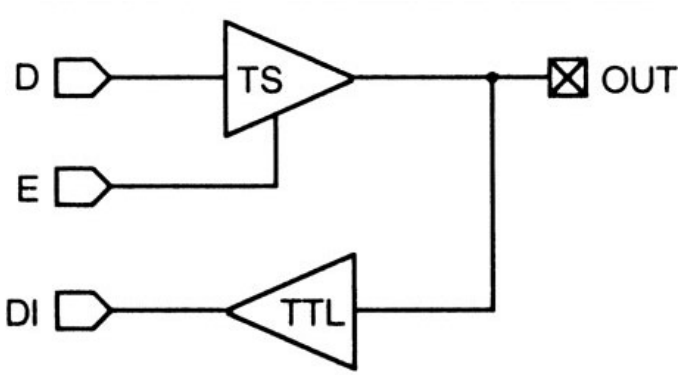
Receiver Circuit for Differential Data



Bidirectional Buffer with TTL Input

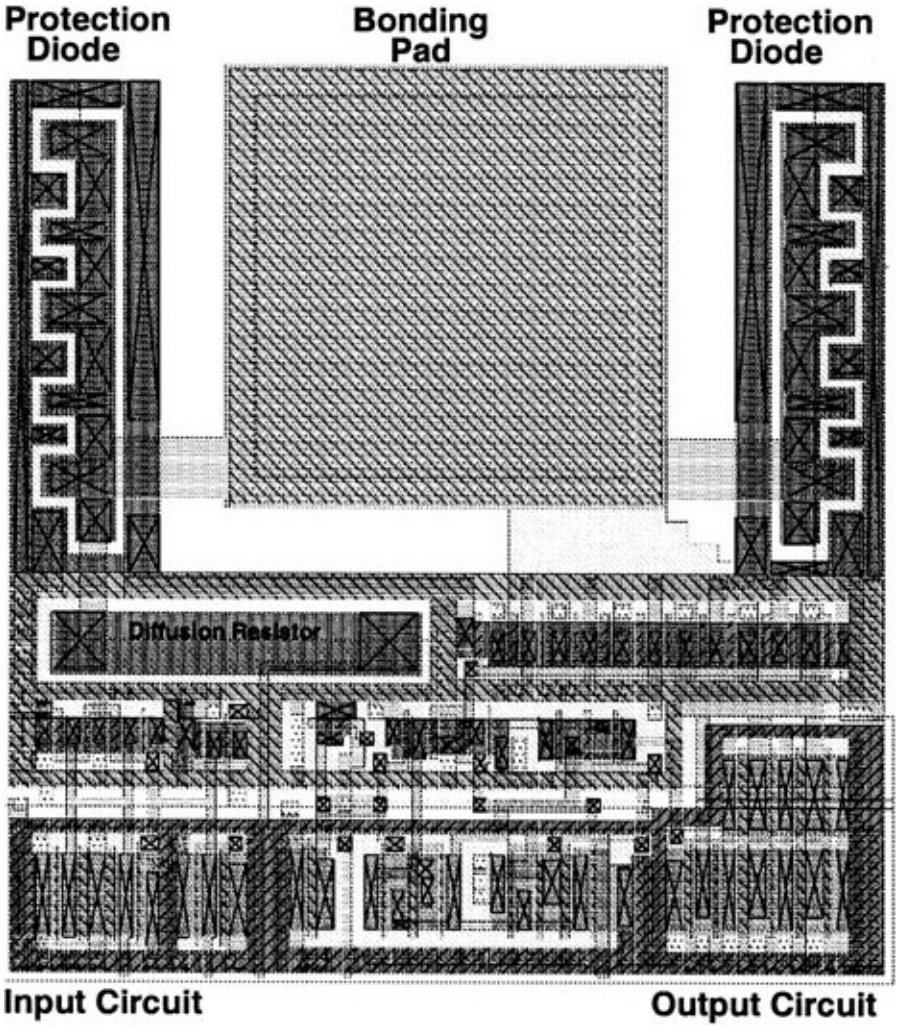


(a) Schematic



(b) Block diagram

Layout of a Bidirectional I/O Pad Circuit

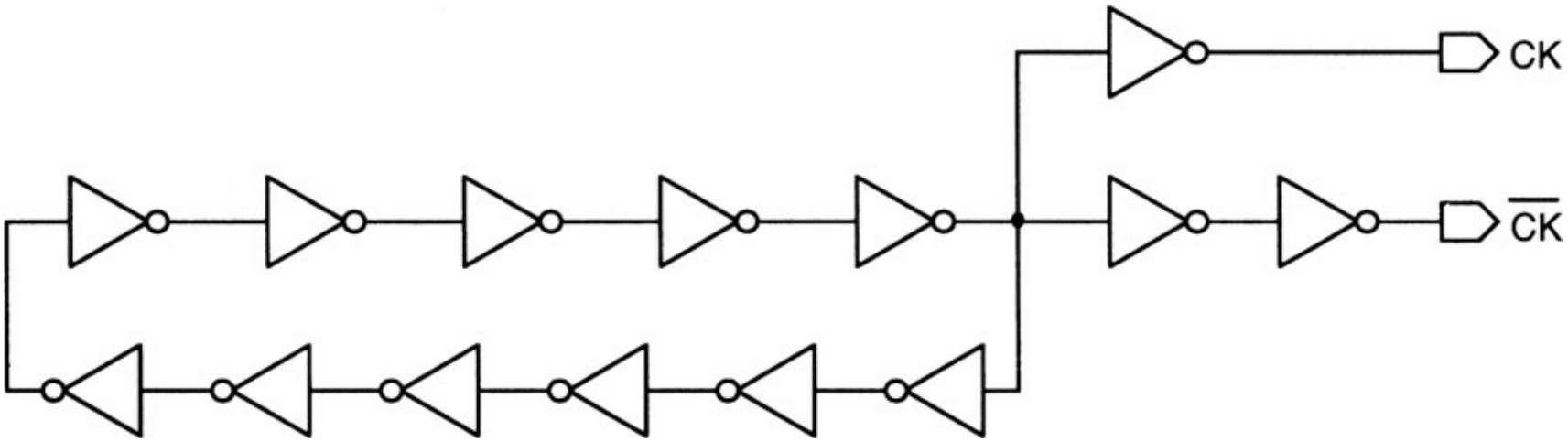


Courtesy of MOSIS

On-Chip Clock Generation and Distribution

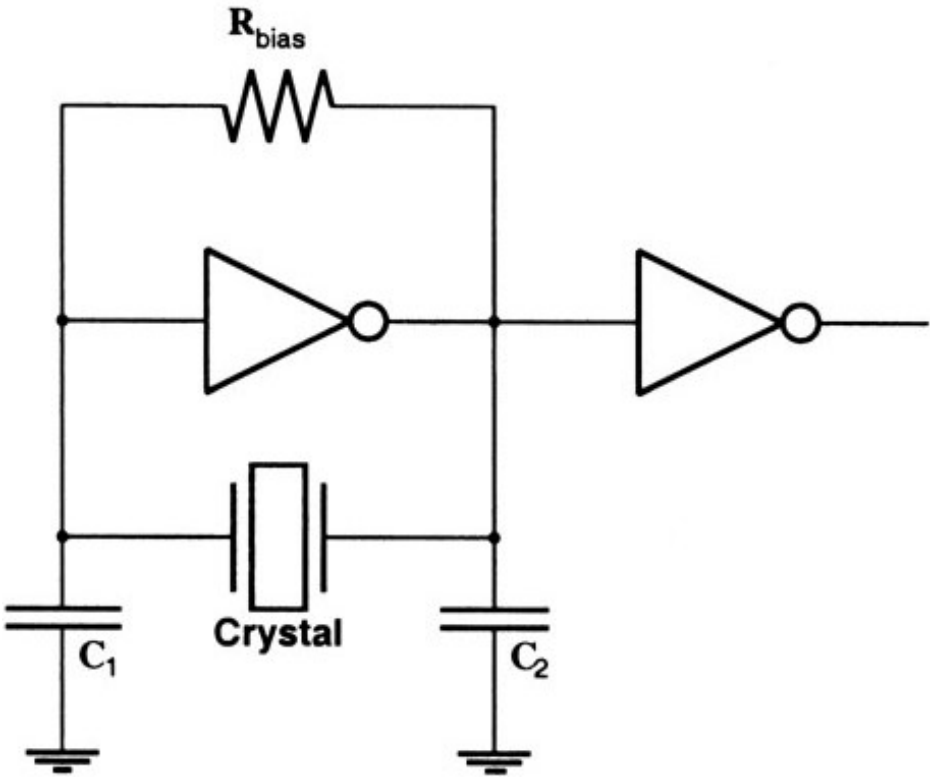
- Clock signal- heartbeats of digital systems
- Skew
  - Spatial clock uncertainty due to PVT variations of clock buffers and interconnect lines in clock distribution network
- Jitter
  - Temporal clock uncertainty from the clock generator and clock buffers
- About 10% of cycle time is expended to allow realistic clock jitter and skews in computer systems

Simple Clock Generator



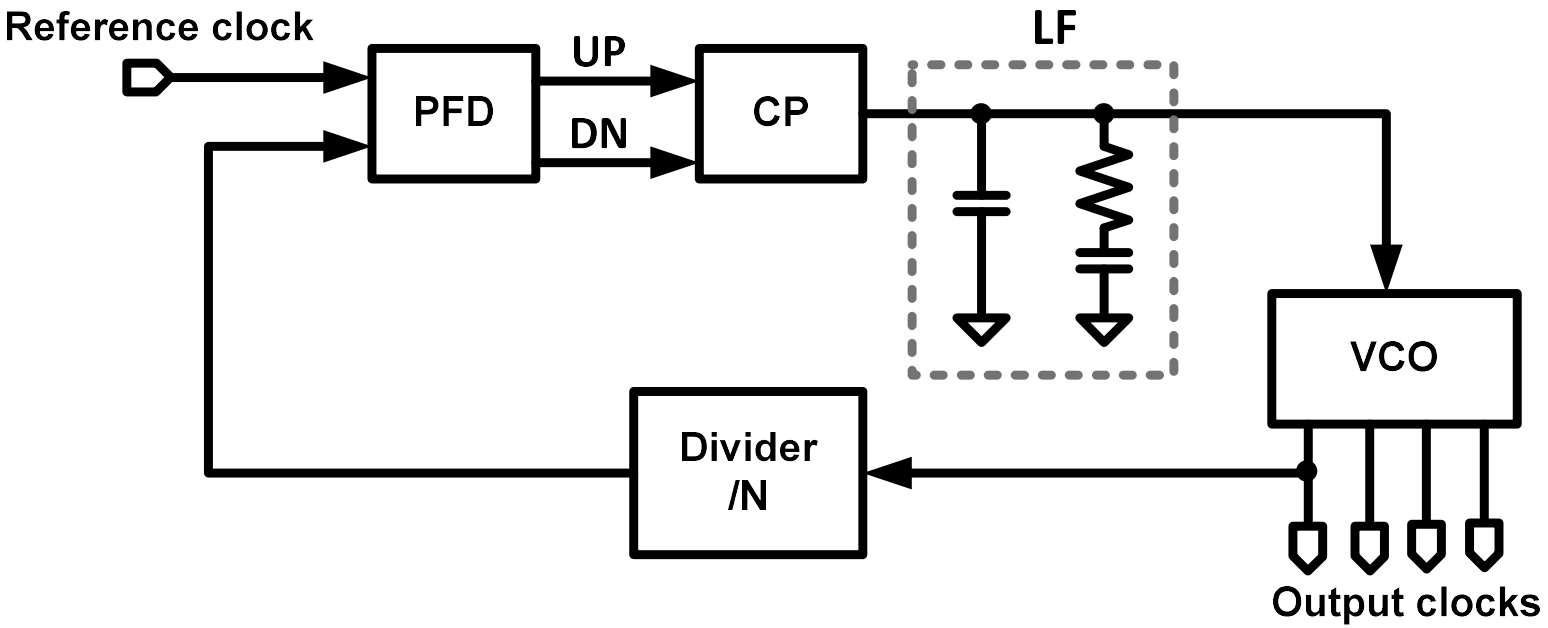
- For low-end microprocessor chips
- Process-dependent
- Unstable

Pierce Crystal Oscillator



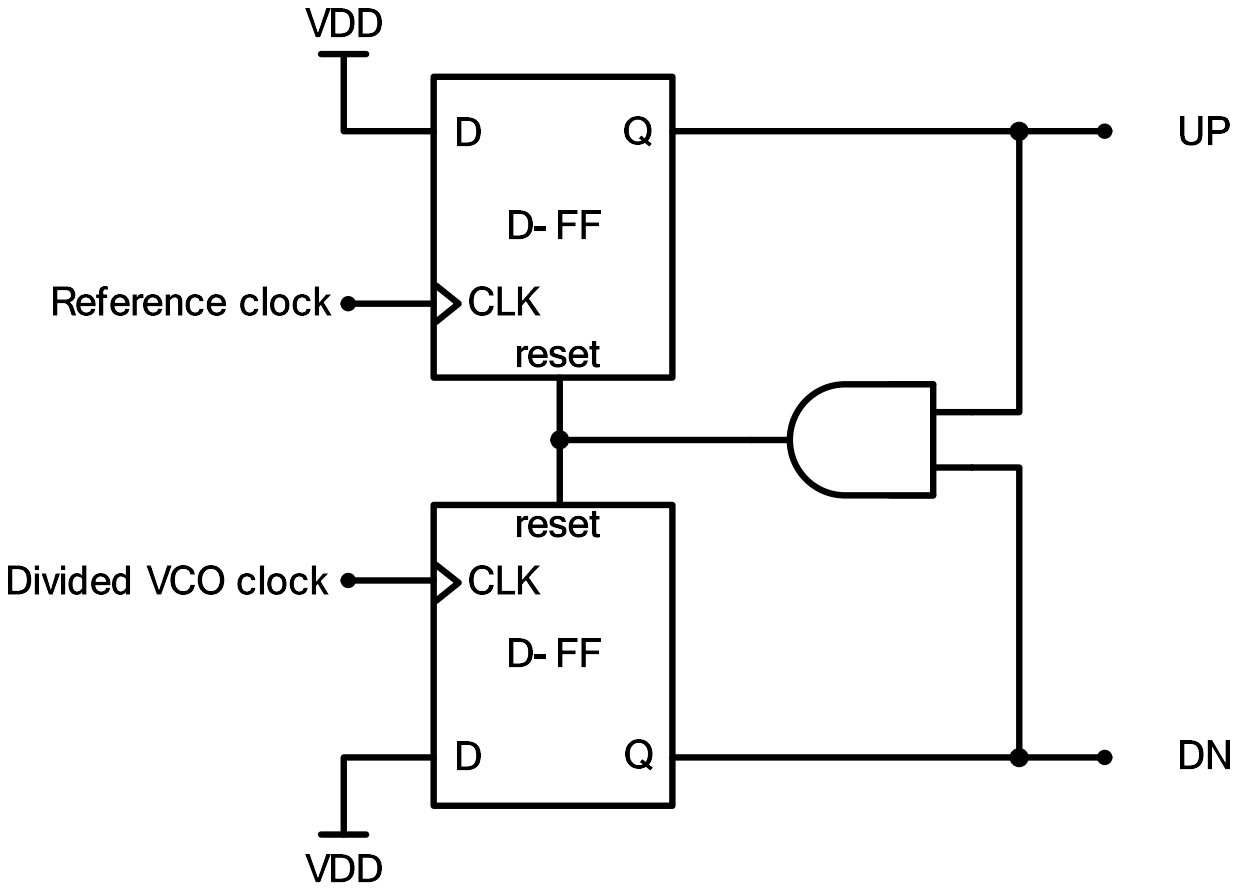
- Good frequency stability
- Near series-resonant circuit
- Internal series resistance and external load
  - determines the frequency and stability
- Internal inverter
  - generates the voltage difference
- External inverter
  - amplify the clock signal

Phase-Locked Loop

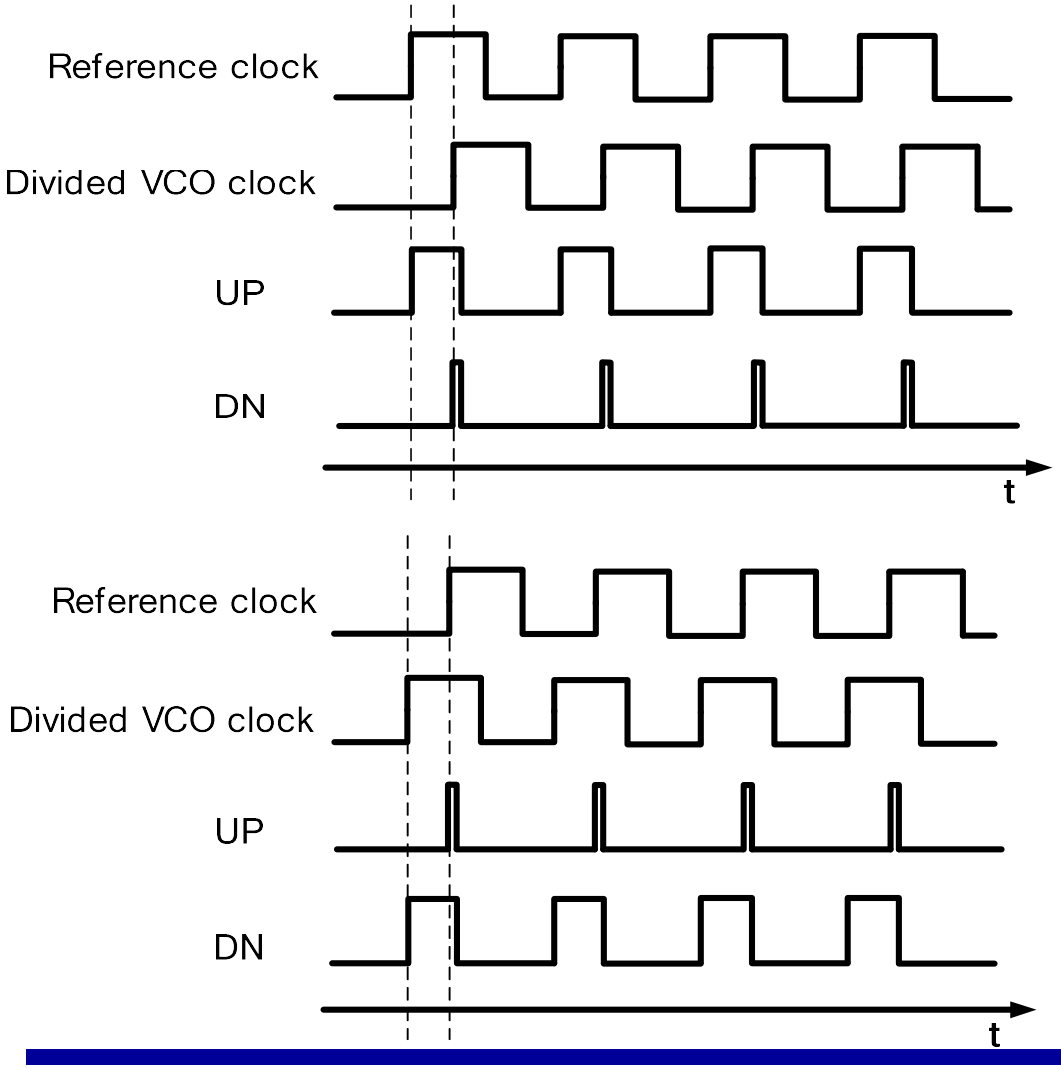


- The most common on-chip clock generator
- Easy multiplication of frequency
  - Frequency of VCO : N times as faster as the reference clock

Phase Frequency Detector(PFD)



Output Pulses of PFD

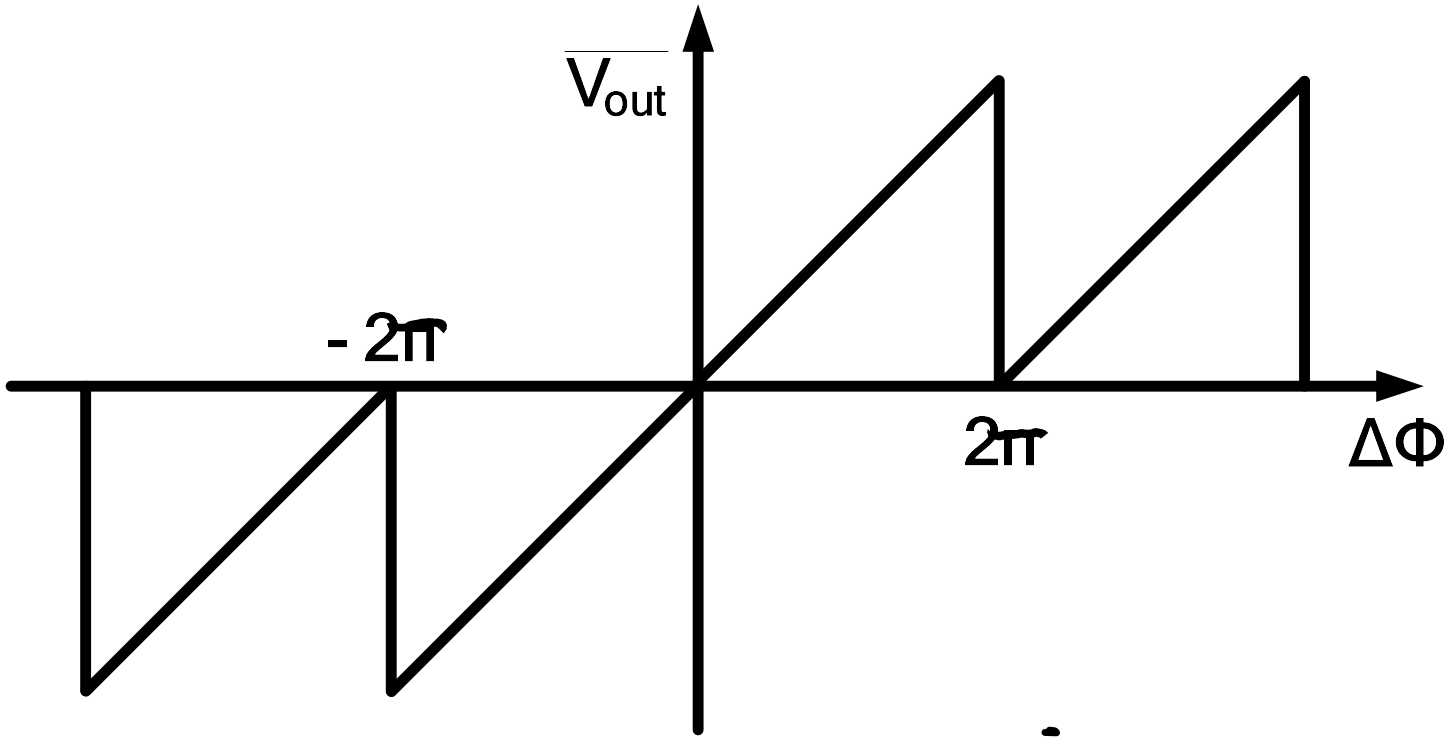


- Reference clock comes faster than the divided VCO clock
  - UP
- The divided VCO clock comes earlier than the reference clock
  - DN

Locked state of PLL

- Locked state of PLL
  - Two clocks come very close
- Dead zone problem
  - If the phase difference of two PFD inputs is as small as few pico seconds, the PFD cannot generate a proper pulse
  - because it takes time for the PFD circuit to respond to the input signals
  - In this case, the pulse width of PFD output would be too small to represent the exact amount of phase error
  - It can be solved by inserting a buffer at the reset path to add some delay

Input and Output Characteristic of PFD



Oscillator

- Oscillator - unstable system that generates repetitive signals
  - Oscillation conditions
    - Loop gain > 1
    - Total phase shift = 360
  - Barkhausen criterion
    - Loop gain, phase shift: $\left|H\left(j\varpi_0\right)\right| \geq 1, \quad \angle H\left(j\varpi_0\right) = 180°$
    - Simple and intuitive
    - Bode plot
    - Necessary but not sufficient to stability
  - Nyquist stability criterion
    - Accurate
    - Root-locus plot

Voltage Controlled Oscillator(VCO)

- VCO
  - Oscillator whose frequency is controlled by the voltage
  - Noise budget of the VCO
    - determines the jitter performance and loop bandwidth of PLL

$$\omega_{out} = \omega_0 + \int K_{VCO} V_{CTRL} dt$$

  - ω_{out} : output frequency
  - ω_0 : initial VCO frequency
  - K_{VCO} : VCO gain
  - V_{CTRL} : VCO control voltage

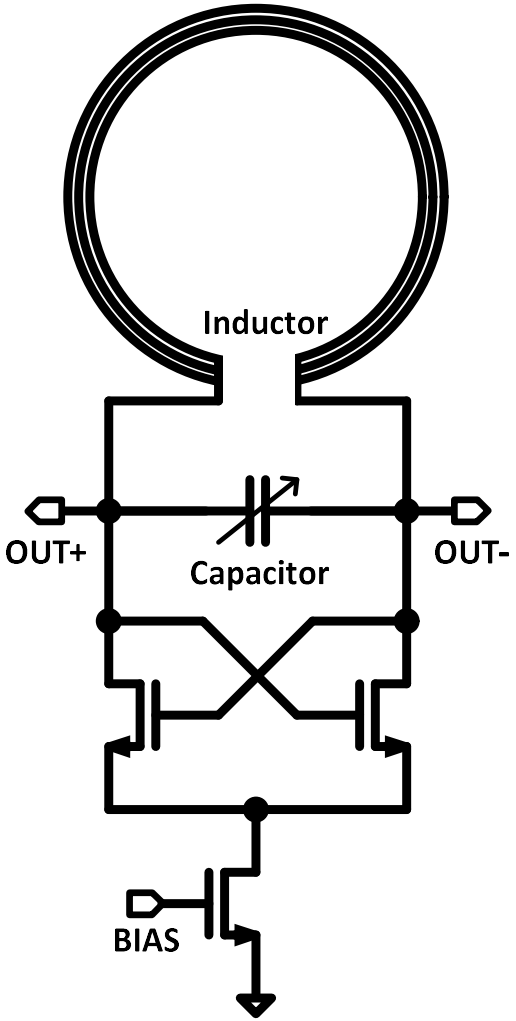
Factors to Consider in VCO (1)

- Free running frequency
  - VCO operating frequency in the absence of control voltage
- Tuning range
  - The range of frequency that VCO can generate
  - It determines the operating range of PLL
- Noise rejection ability
  - A measure of how much noise from external environment the VCO can filter out
  - Supply noise rejection / Common-mode noise rejection

Factors to Consider in VCO (2)

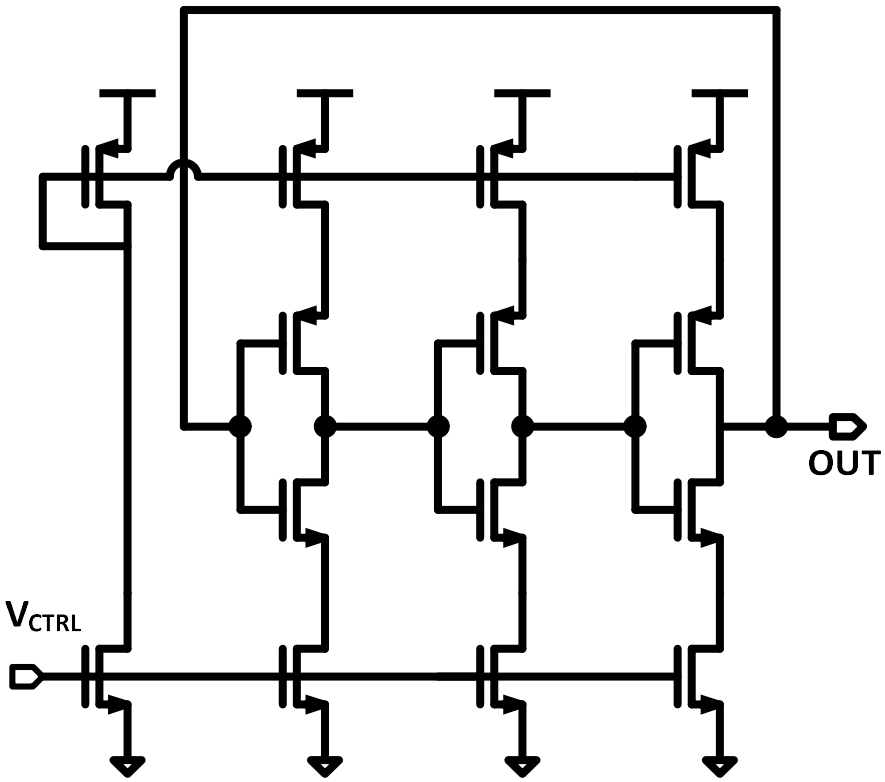
- Power consumption
  - Critical to low-power applications
  - The more power, the better jitter performance
- Output signal purity
  - The most important factor
  - Clock jitter / phase noise

Harmonic Oscillator



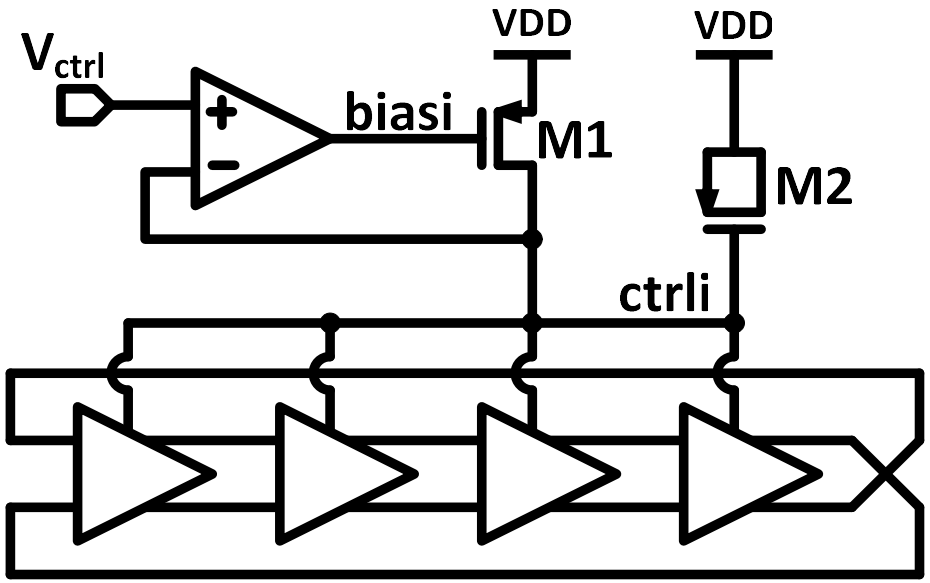
- Resonance of the energy components such as LC-tank
- Good signal purity
- But bulky (inductor and capacitor)
- Tuning range – narrow
- Not suitable for digital systems

Relaxation Oscillator



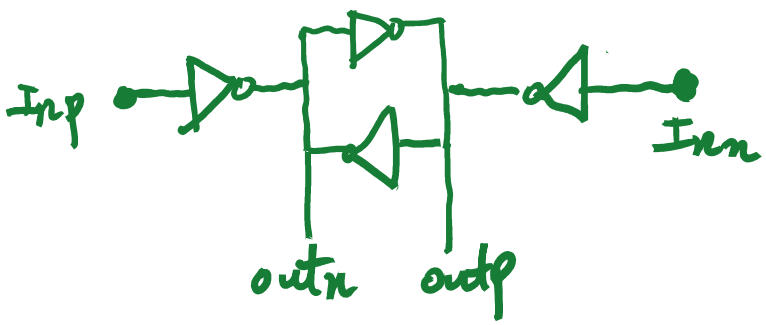
- Chain of delay elements
- Easy to design
- Compact size
- Bad signal purity
- Typical example: ring oscillator

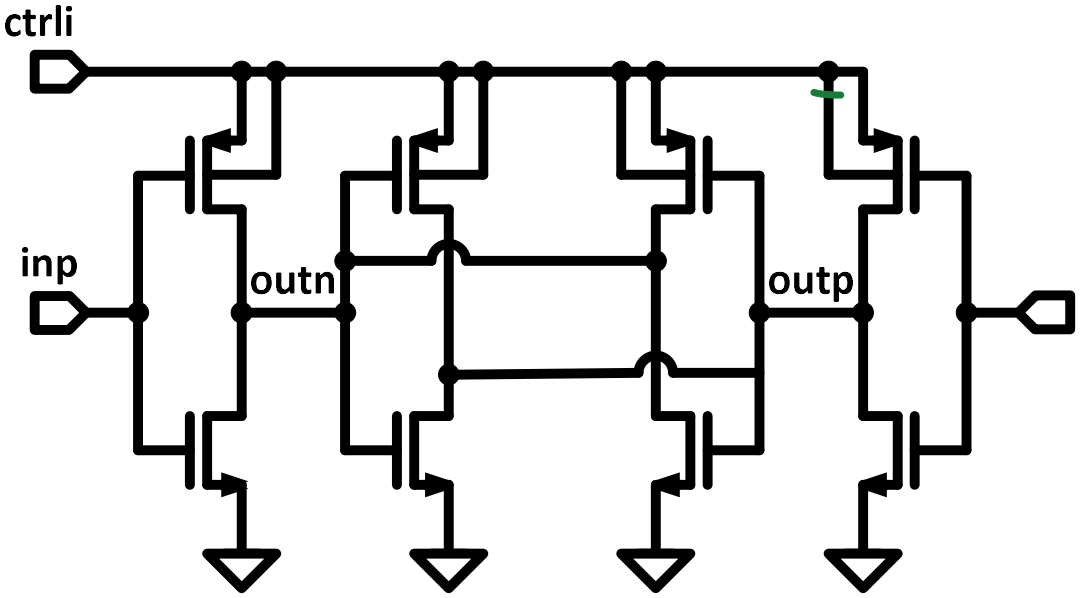
VCO with Supply Noise Rejection



- Regulated voltage ctrli
  - robust to supply noise
- Opamp BW > PLL BW
- M1: large
  - Enough voltage headroom
  - Wide operating range of VCO
- M2: suppress ripples on ctrli
- Dominant pole on node ctrli
  - Compensation capacitor and resistor are needed between node biasi and ctrli

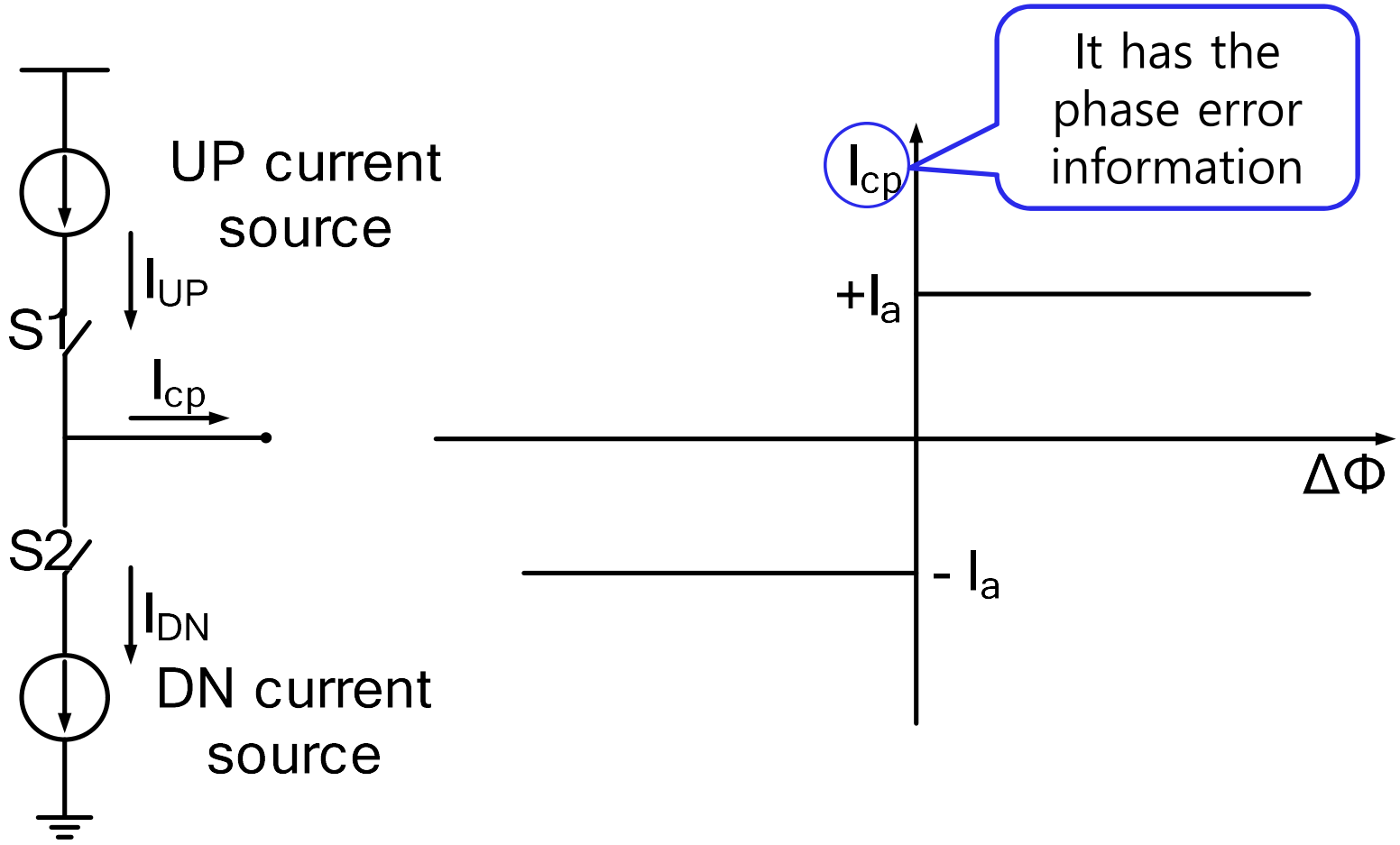
Delay Cell





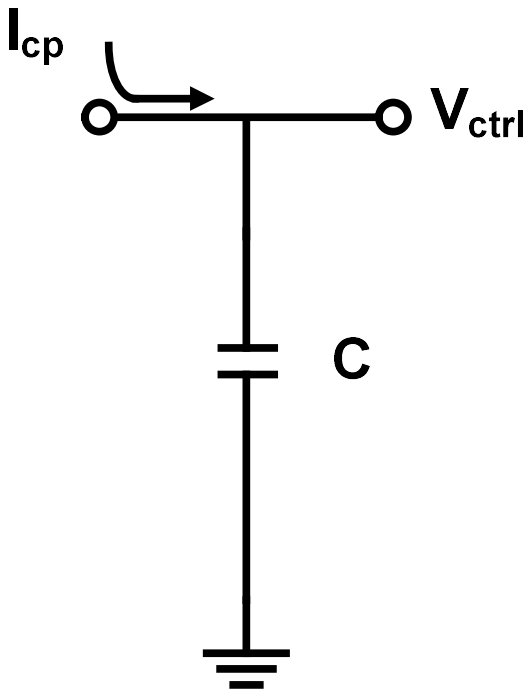
- Pseudo-differential type
- Back-to-back inverters are used
- ctrli controls the delay
- Body of PMOS is tied to the source
  - Linear change in frequency

Charge Pump(CP)

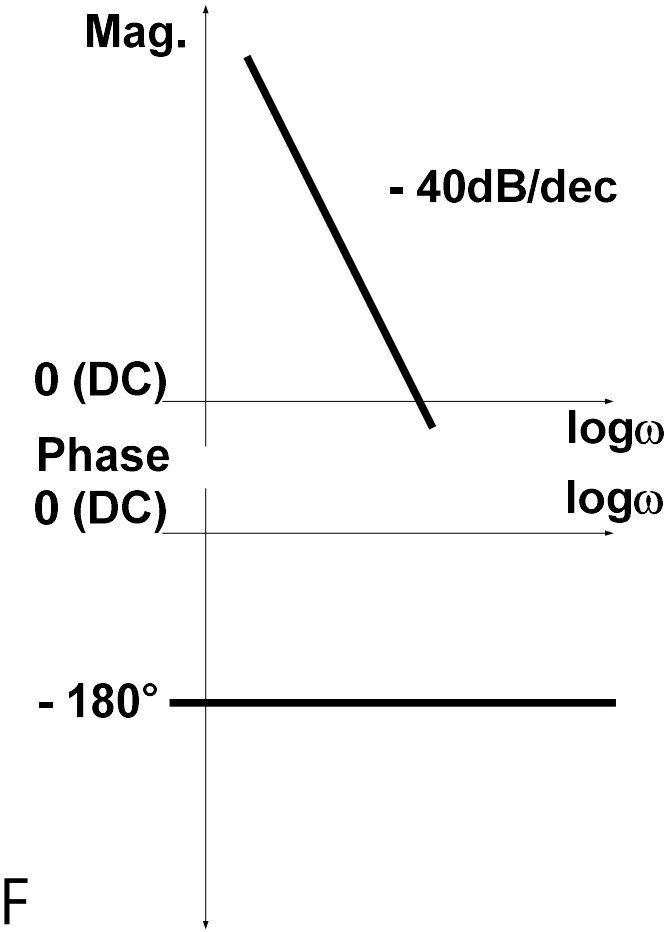


(a) Conceptual structure (b) Ideal output current of CP

Loop Filter (1)

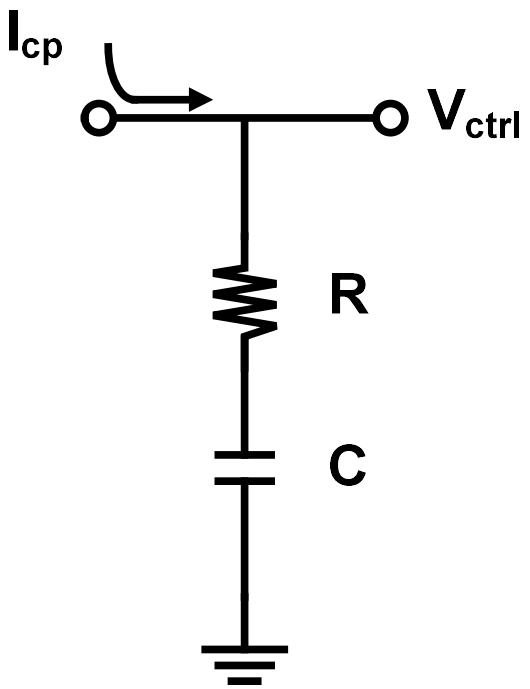


$$\frac{V_{ctrl}}{I_{cp}} = \frac{1}{sC}$$

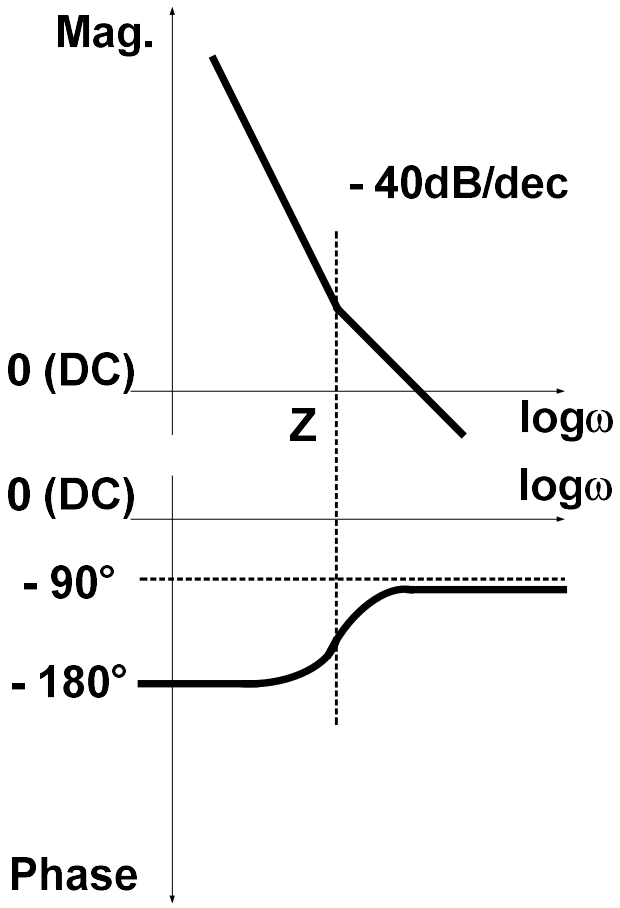


- Loop Filter(LF) converts current from CP to voltage
- One pole at VCO, the other pole at LF
  - Two poles at DC -> Unstable

Loop Filter (2)

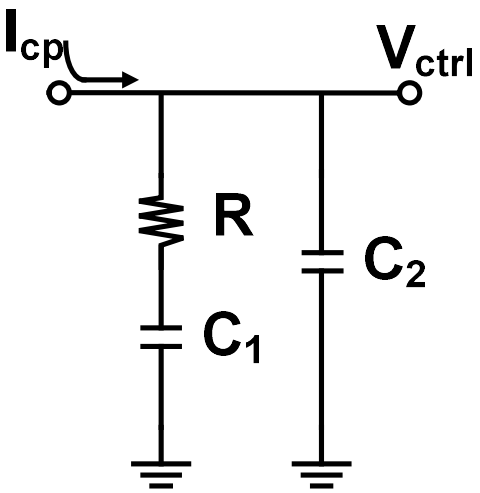


$$\frac{V_{ctrl}}{I_{cp}} = R + \frac{1}{sC} = \frac{sRC+1}{sC}$$



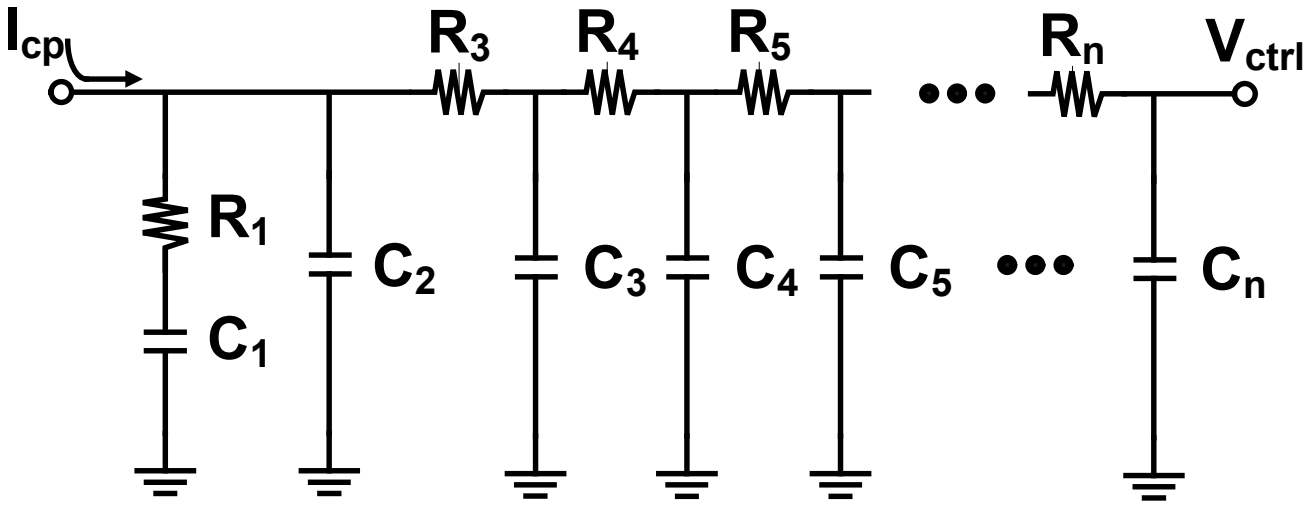
- Additional resistor introduces zero for larger phase margin

Loop Filter (3)



$$\frac{V_{ctrl}}{I_{cp}} = \left(R + \frac{1}{sC_1}\right) \| \left(\frac{1}{sC_2}\right) = \frac{sRC_1}{s^2RC_1C_2 + s(C_1 + C_2)}$$

- C_2 reduces fluctuation caused by the IR drop



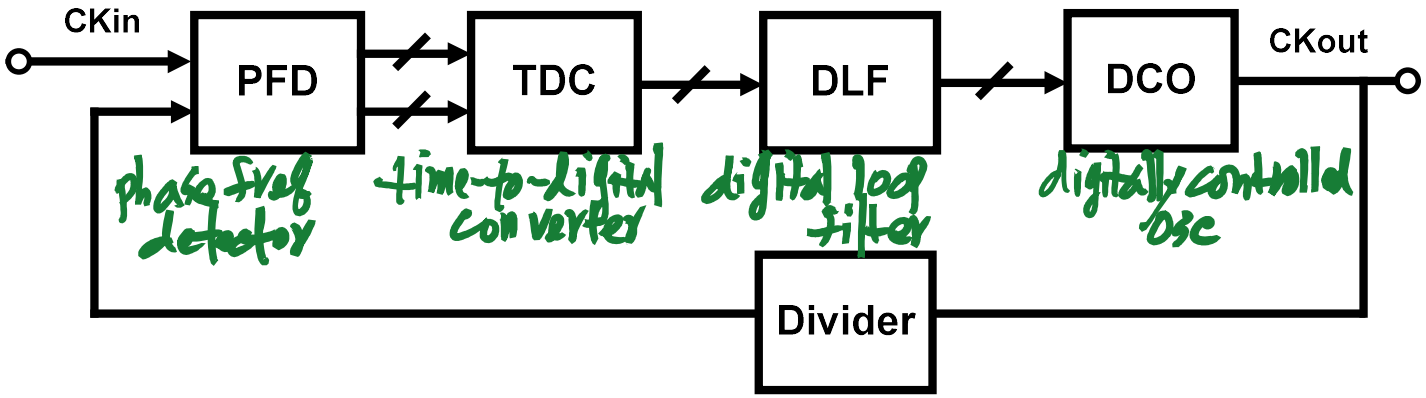
- Higher order LF
  - Filters out noise
  - Vctrl < Vcp =>Narrow range

All-Digital PLL(ADPLL)

- Issues in analog PLL in deep-submicron process

  - Leakage current in capacitors
  - Steady-state power consumption
  - Long-term jitter
  - Small supply voltage
  - High threshold voltage

→ Narrow PLL operating range, high PLL noise sensitivity



- ADPLL is introduced

Components of ADPLL

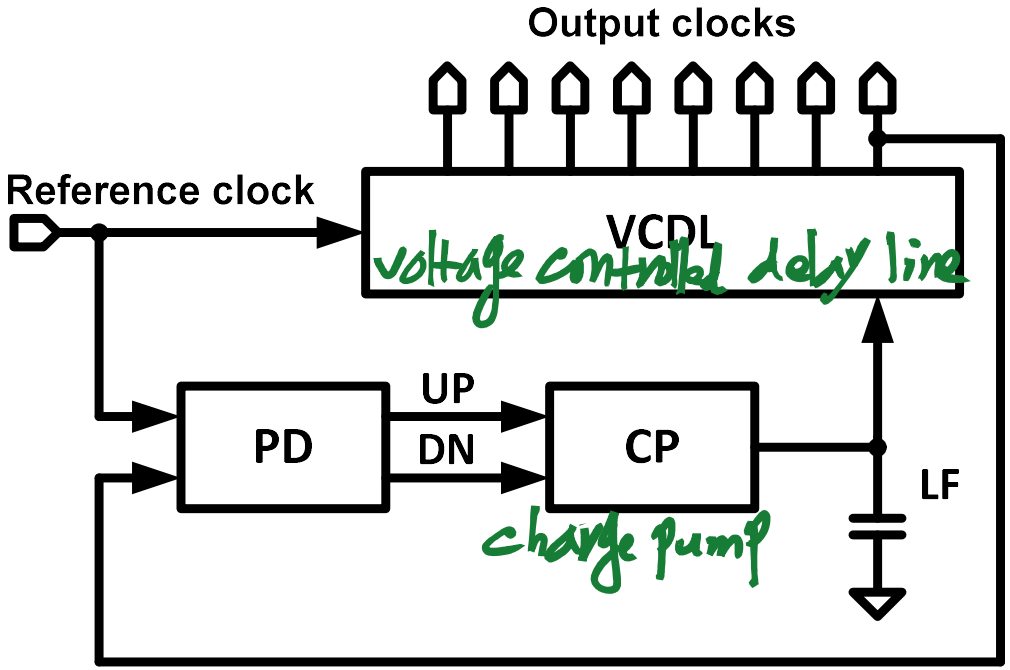
- Phase-Frequency Detector(PFD)
- Time-to-digital converter(TDC)
  - converts phase difference to digital words
  - replaces CP
- Digital loop filter(DLF)
  - filters out digital input words
- Digitally controlled oscillator(DCO)
  - replaces a VCO

Advantage/Disadvantage of ADPLL

- Advantage
  - Excellent timing accuracy
  - No analog circuits that suffer from small voltage headroom and relatively high threshold voltage
  - Robust to PVT variation
    - Only TDC and DCO are sensitive
  - Good for deep-submicron processes

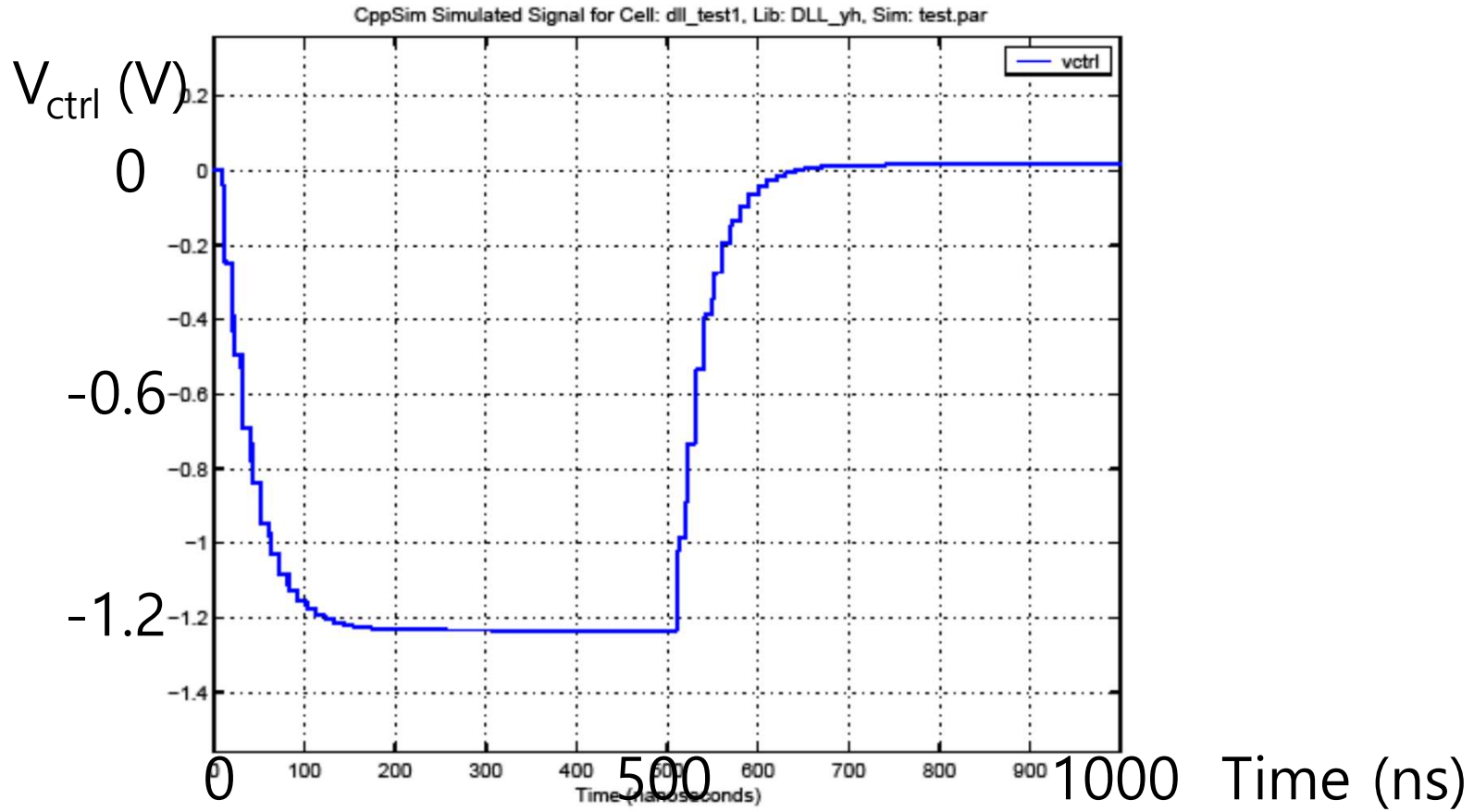
- Disadvantage
  - Limited resolution in phase detection by TDC
  - Small resolution in frequency control by DCO
  - Possibly more jitter than analog PLL

Delay-Locked Loop(DLL)



- VCDL adjusts the delay by a control voltage
- DLL adjusts the phase of VCDL / PLL modifies the frequency
- PLL has one more pole than DLL (2^{nd}-order)
- No stability issue in DLL

Simulation of DLL Locking Process

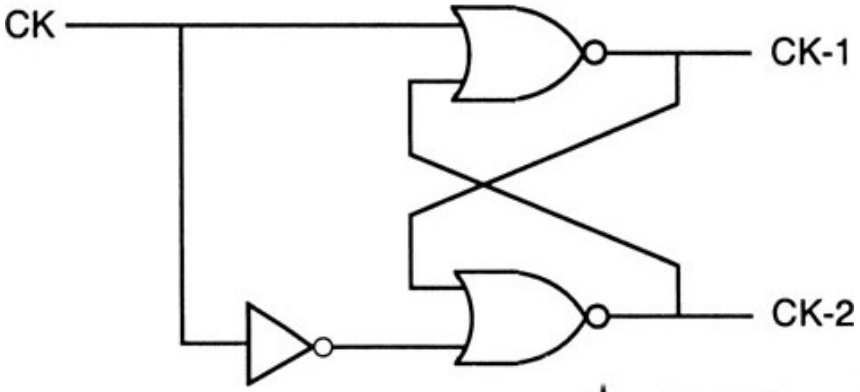


- V_{ctrl} changes when abrupt phase shift occurs at 0ns and 500ns

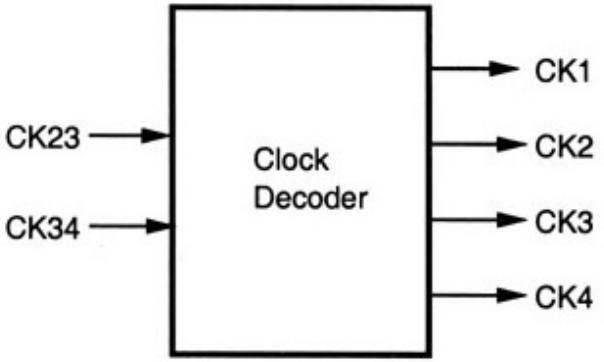
Comparison of PLL and DLL

PLL	DLL
VCO-Jitter accumulation	VCDL–No jitter accumulation
Higher-order system - Can be unstable - Hard to design	1st-order system - Always stable - Easier to design
Costly to integrate LF	Easier to integrate LF
Less Ref. signal dependent	Ref. signal dependent
Easy Freq. multiplication	Difficult Freq. multiplication
No limited locking range	Limited locking range $T_{Ref} < VCDL_{delay} < 3T_{Ref}/2$
EMI problem	Less EMI Problem

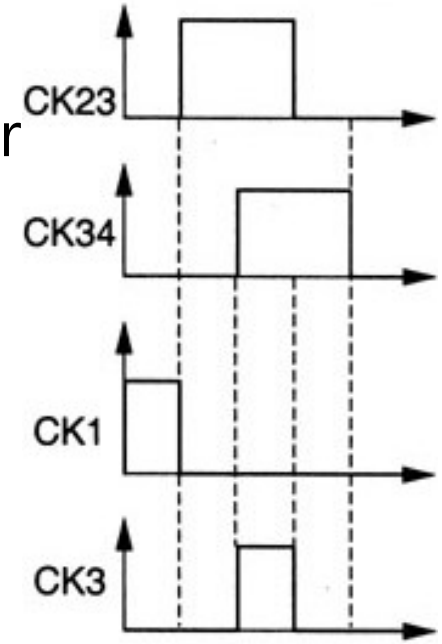
Non-overlapping Clock Generator



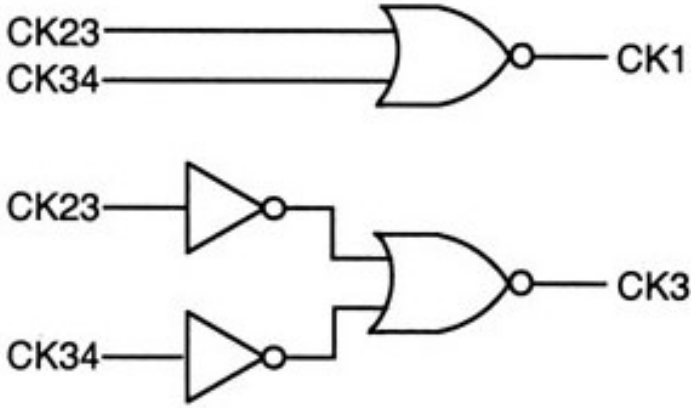
- Two phase clock generator



- Clock decoder symbol

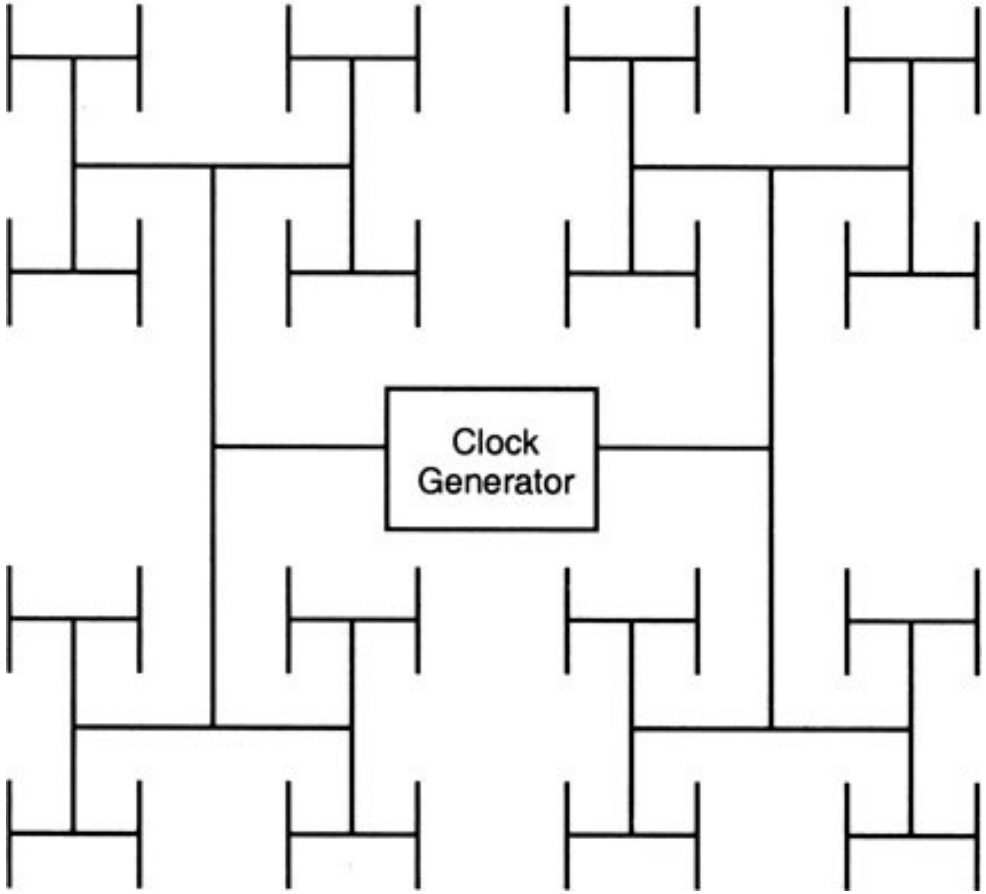


- Clock decoder waveform



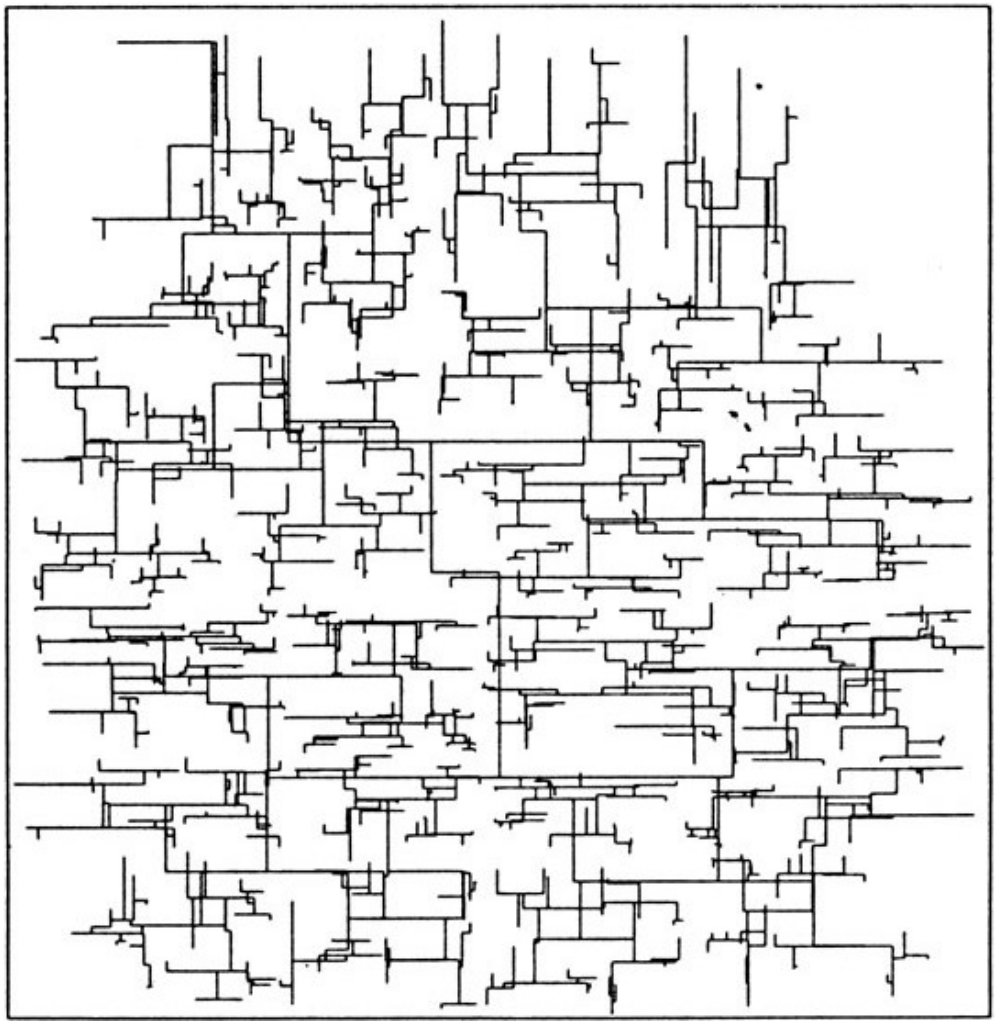
- Clock decoder schematic

Uniform Clock Distribution(H-tree)



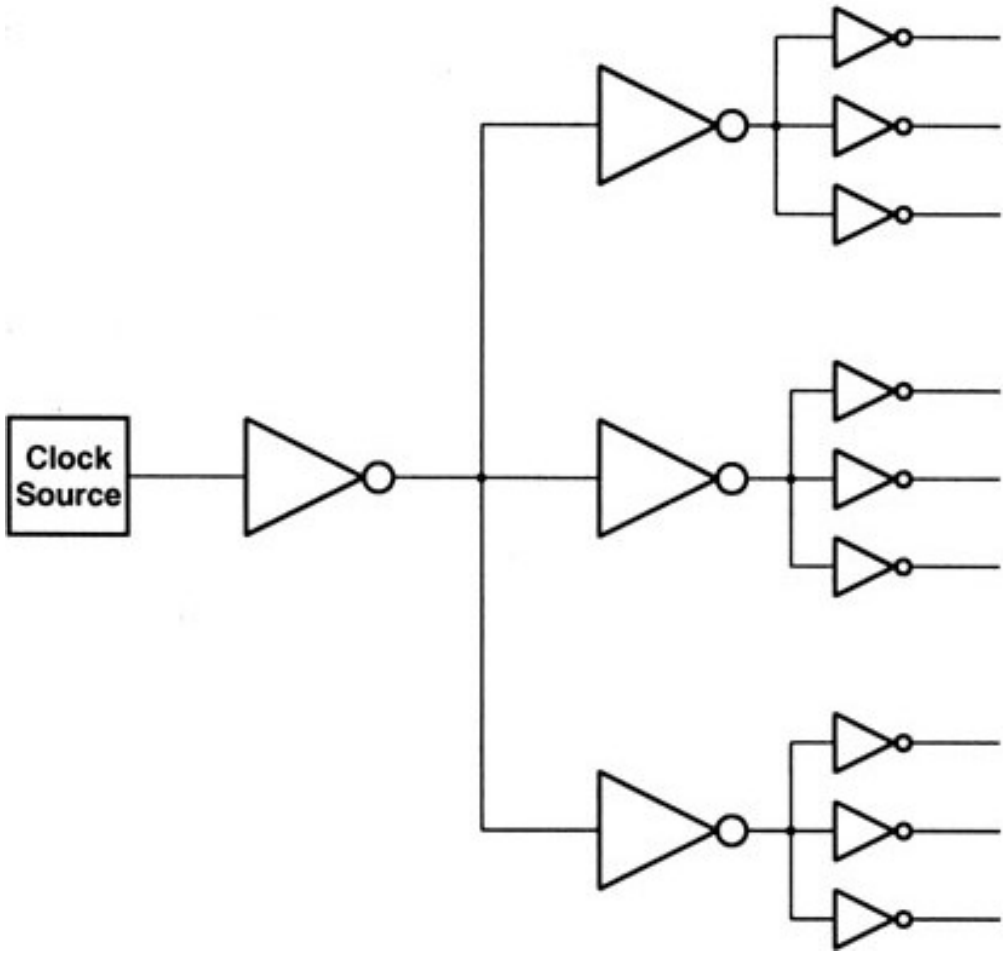
- All clock signals are distributed with a uniform delay
- Difficult to achieve due to constraints of routing and fanout

Zero-Skew Network By CAD



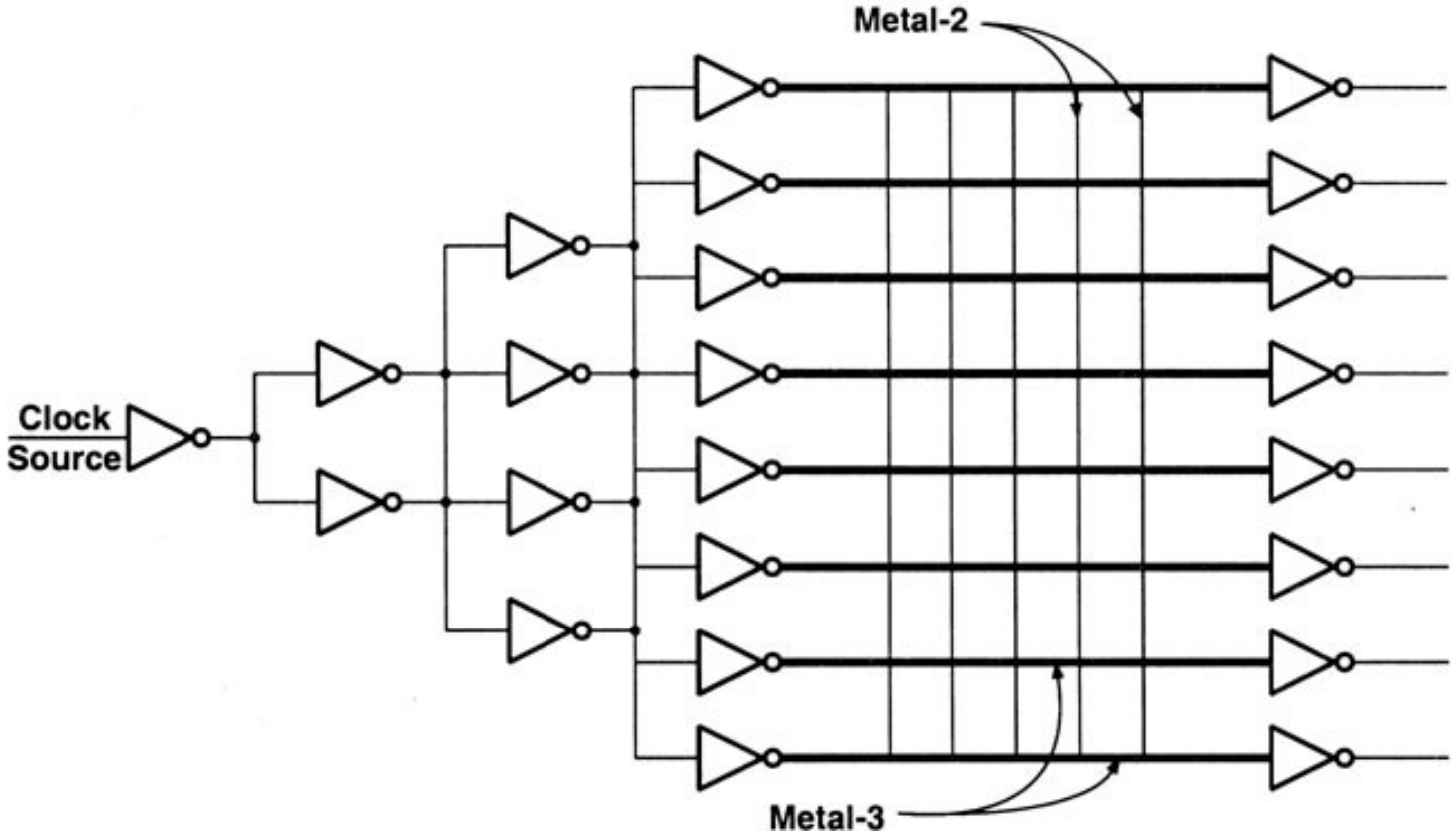
- An example of the zero-skew clock routing network, generated by a computer-aided design(CAD) tool

Buffered Clock Distribution Network



- Every stage has the same number of fan-outs
- Essential for the balanced clock delays

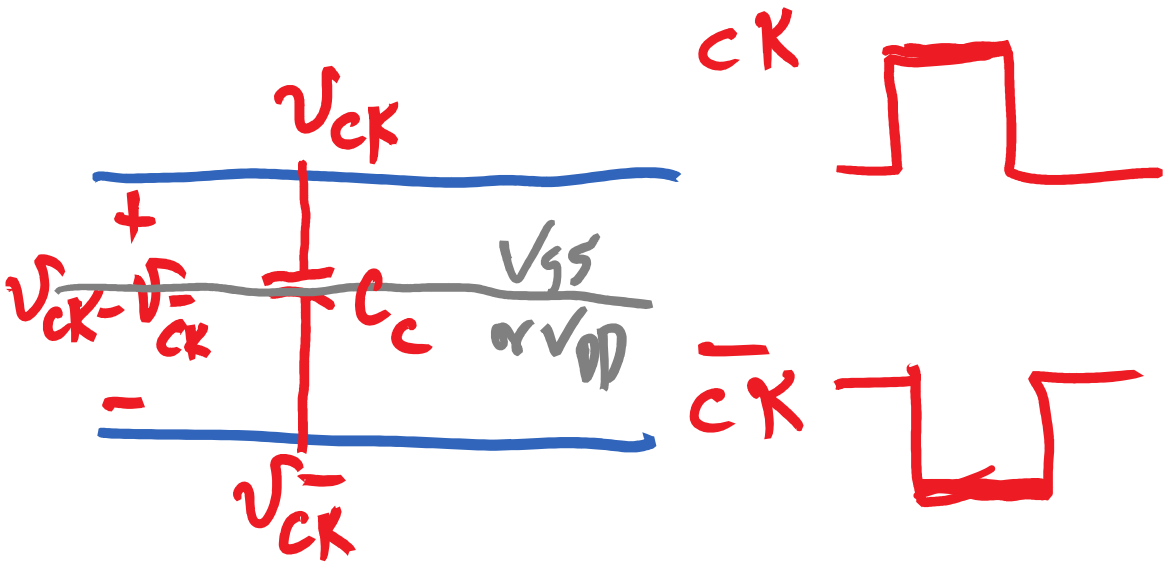
Clock Distribution in the DEC Alpha Chip



- Mesh pattern of interconnect wires
- Clock signals are kept in phase across the entire chip

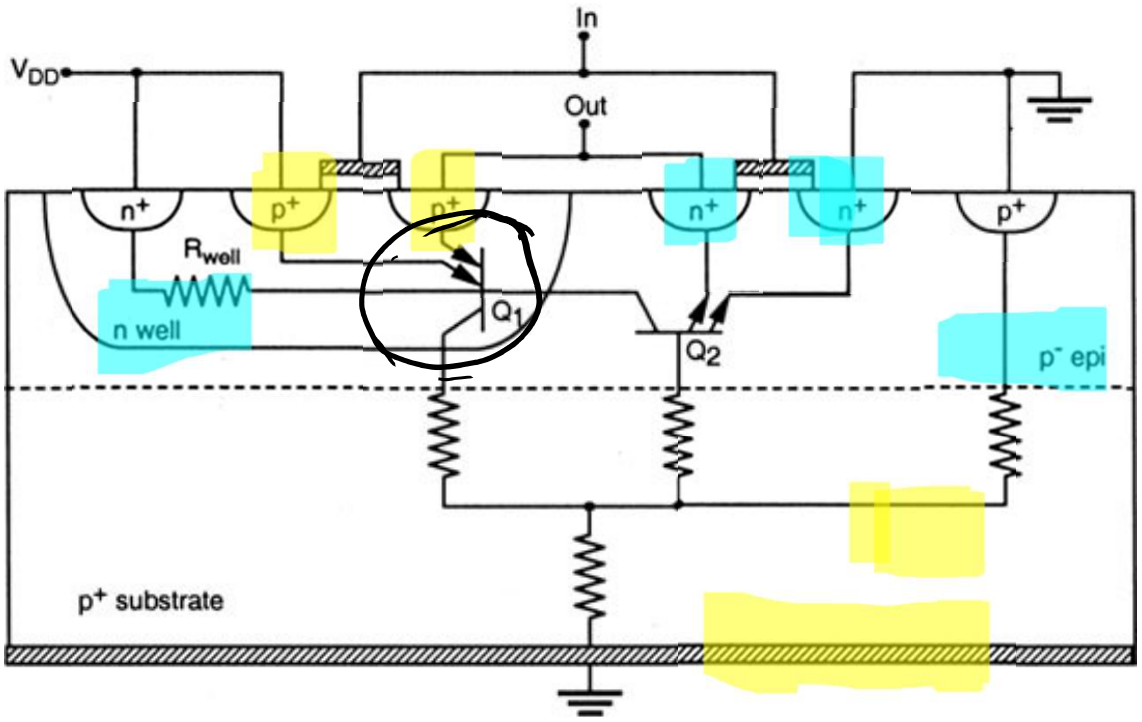
Considerations For VLSI Design

- Ideal duty cycle of a clock = 50%
- Feedback based on the voltage average improves the duty
- t_r and t_f should not be reduced excessively for prevention of reflection in the interconnection network
- Small load cap reduces the fan-out, the interconnect lengths, and the gate capacitances
- Small impedance of clock line by increasing the (*w/h*) ratios (the ratio of the line width to vertical separation distance of the line from the substrate)
- Cross-talk prevention
  - Adequate separation between clock lines
  - Power or ground rail between high-speed lines



$C_c \frac{dV_c}{dt} \Rightarrow 2C_c$ Miller effect

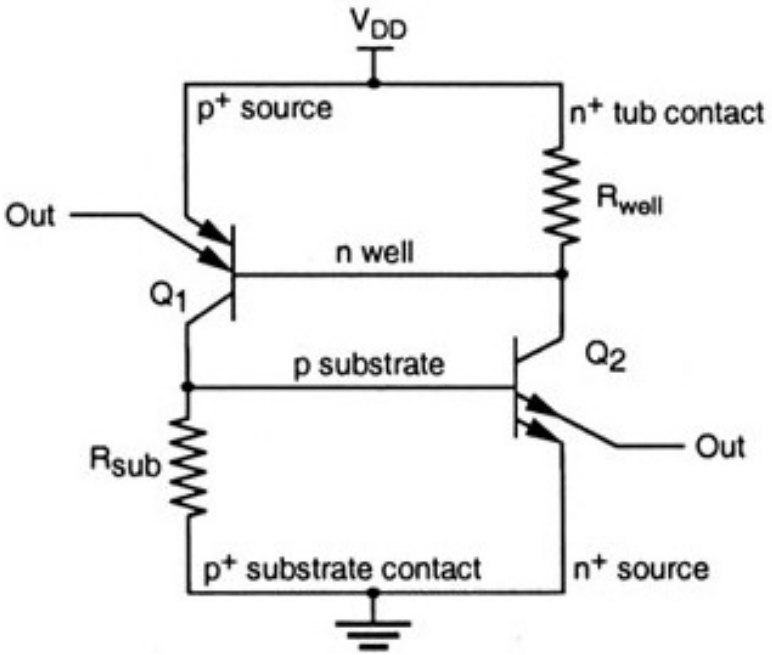
Latch-Up (1)



Cross-sectional view

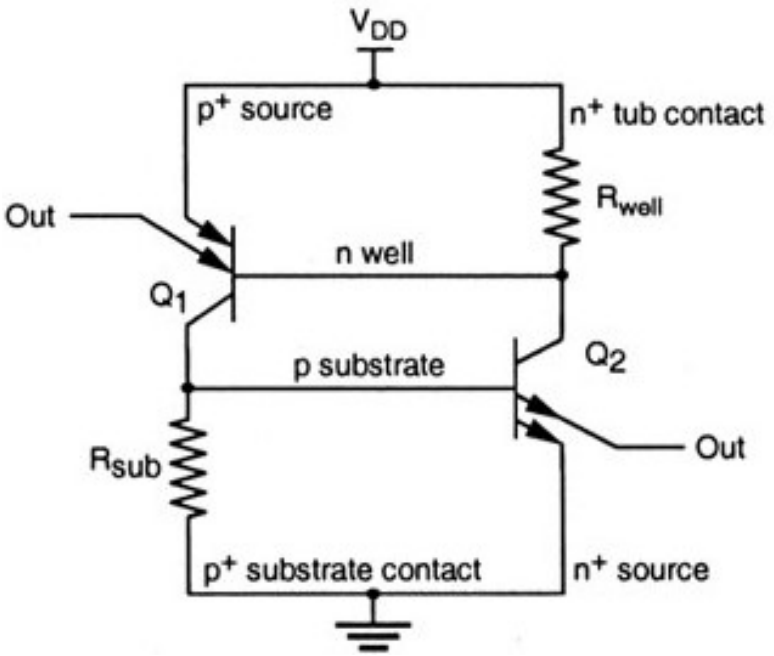
- Silicon-controlled rectifier(SCR) with positive feedback
- Excessive current flow -> device damage
- Concerns of esp. I/O circuits

Circuit Model of Latch-Up



- R_{well}: 1kΩ~20kΩ
- R_{sub}: a few Ω~several hundred Ω
- Assumption
  - R_{well} and R_{sub} are large enough to be neglected (open circuit)
- Initial condition
  - Current gain: very low
  - Only reverse leakage currents flows

Triggering the Latch-Up



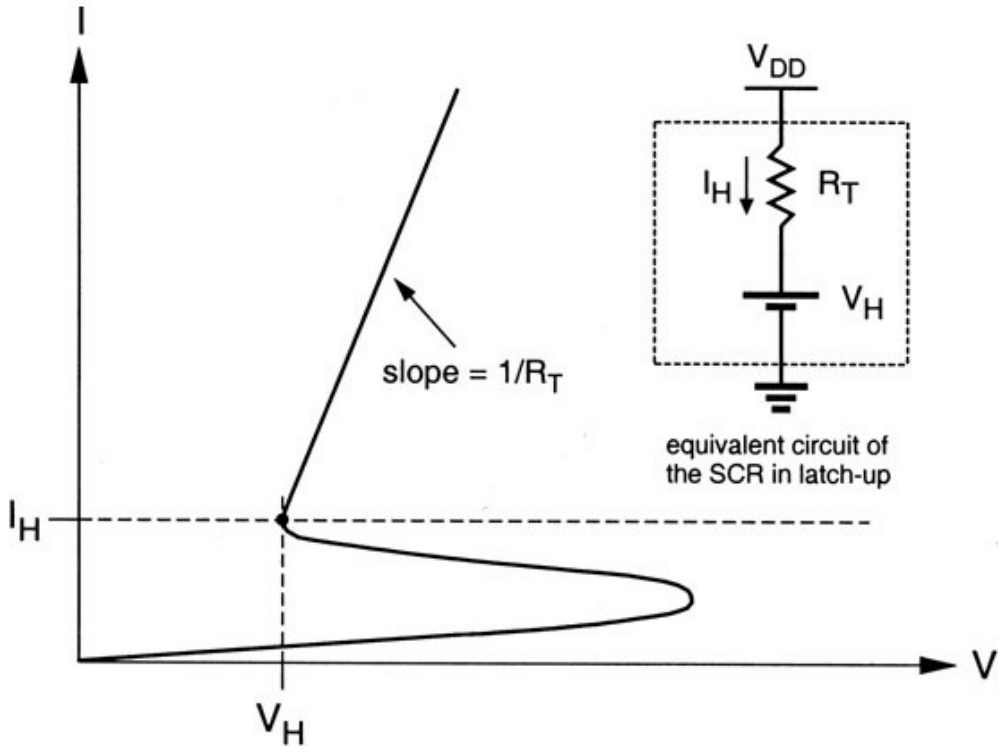
- Trigger process
  - I_C of one of BJTs is increased by an external disturbance
  - Feedback loop multiplies it by (β1· β2) -> positive feedback
  - Low-impedance path is formed
- Trigger condition

$$\beta_1 \cdot \beta_2 \geq 1$$

  - Or

$$\frac{\alpha_1}{1-\alpha_1} \cdot \frac{\alpha_2}{1-\alpha_2} \geq 1 \quad \Rightarrow \quad \alpha_1 + \alpha_2 \geq 1$$

Current-Voltage Characteristics of a SCR



- Voltage drop across the SCR in latch-up

$$V_H = V_{BE1,sat} + V_{CE2,sat}$$
$$= V_{BE2,sat} + V_{CE1,sat}$$

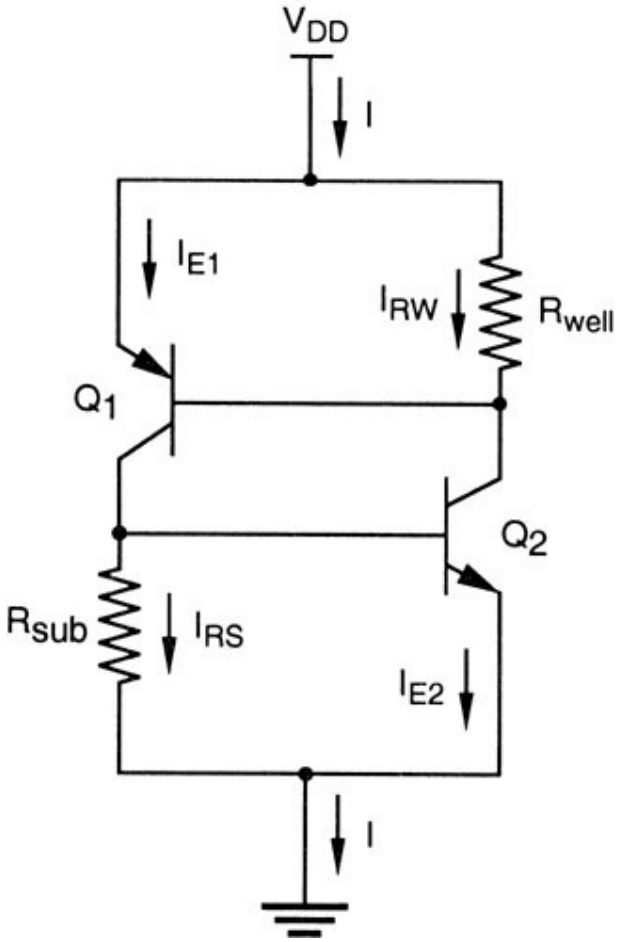
  - V_H : holding voltage
  - I_H : holding current
    - Low impedance state if $I > I_H$

- R_T : total parasitic R in the current path

Causes for Latch-Up

- Large slew rate of VDD during initial start-up
  - Displacement currents
    - By well junction capacitance in the substrate and the well
  - *Dynamic recovery* if the slew rate is not very high
- I/O signal swing much over VDD or far below VSS
  - By impedance mismatches in transmission lines
- ESD stress
  - Minority carrier injection: clamping device → substrate or well
- Sudden transients in buses
  - Due to simultaneous switching of many drivers
- Leakage currents in well junctions
- Radiation of X-rays, cosmic rays, or alpha particles

Derivation of I_H (1)



- From left figure,

$$I = I_{E1} + I_{RW}$$

$$I = I_{E2} + I_{RS}$$

- From relations of Q1 and Q2,

$$I_{C1} = \alpha_1 I_{E1} = \alpha_1^0 I$$

$$I_{C2} = \alpha_2 I_{E2} = \alpha_2^0 I$$

- α_1^0, α_2^0 : equivalent collector-to-emitter current gains absorbing the effects of parasitic R into TRs

- The SCR current I,

$$I = I_{C1} + I_{C2} + (I_{CBO1} + I_{CBO2})$$

Derivation of I_H (2)

- From above equations,

$$I = \frac{I_{CBO} - (I_{RS}\alpha_1 + I_{RW}\alpha_2)}{1-(\alpha_1 + \alpha_2)}$$

- I_H is defined as the current with zero I_{CBO}

$$I_H = \frac{I_{RS}\alpha_1 + I_{RW}\alpha_2}{\alpha_1 + \alpha_2 - 1}$$

- If $\alpha_1 + \alpha_2$ is close to 1, I_H will be large
- The SCR current at the onset of latch-up,

$$I \geq I_H = (V_{DD} - V_H)/R_T$$

Latch-Up Condition

- Both transistors are at the saturation boundary

$$V_H = 2V_{BE} \text{ with } V_{BE1} = V_{BE2} = V_{BE}$$

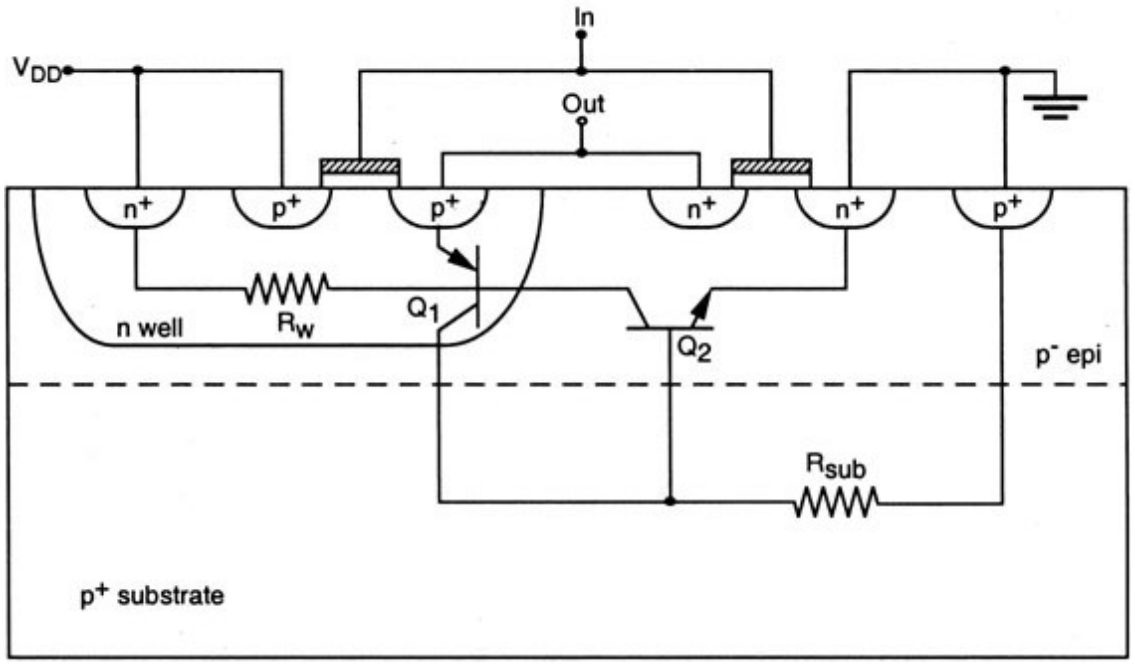
$$I_{RW} = V_{BE} / R_{well} \text{ and } I_{RS} = V_{RE} / R_{sub}$$

- Therefore, the condition for latch-up is

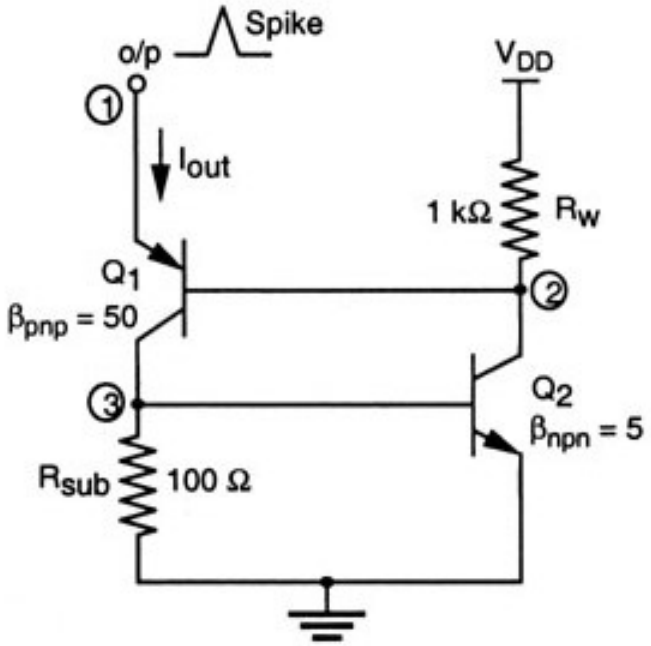
$$\alpha_1 + \alpha_2 \geq 1 + \left(\frac{\frac{R_T}{R_{well}}\alpha_1 + \frac{R_T}{R_{sub}}\alpha_2}{\frac{V_{DD}}{V_{BE}} - 2} \right)$$

- Above inequality shows that small R_{sub} and R_{well} help avoiding the latch-up

Simulation of Latch-Up (Schematic)

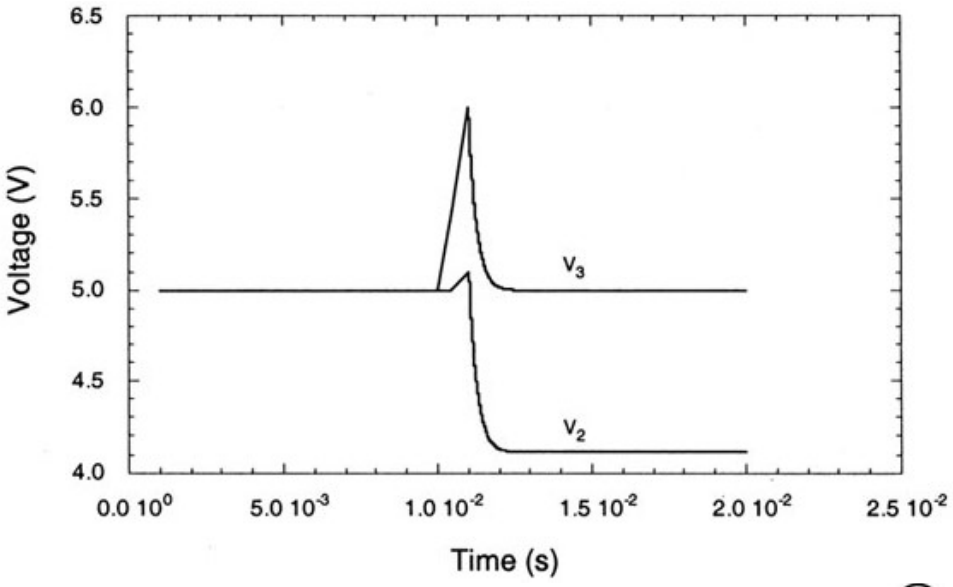


(a) CMOS inverter with parasitic BJTs



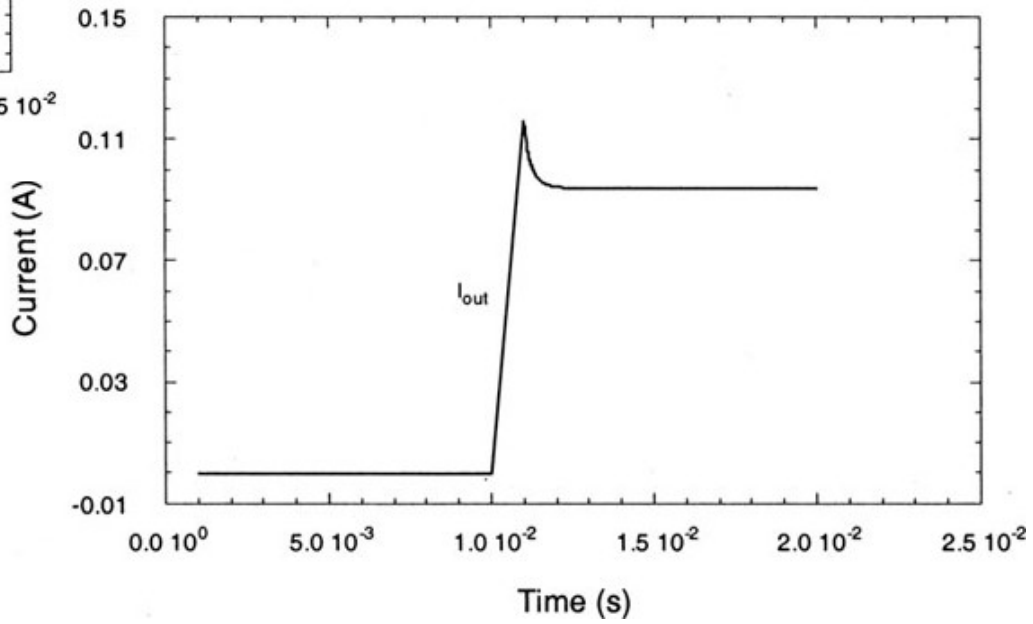
(b) Schematic of the simulation

Simulation of Latch-Up (Waveform)



(a) Voltage

(b) Current



Latch-Up Guidelines(1)

- Gold doping of the substrate
  - Reduce gains of BJTs by lowering the minority carrier lifetime
- Schottky source/drain contacts
  - Reduce the minority carrier injection efficiency of BJT emitters
- Guardband rings: capture the injected minority carriers
  - P+ guard rings connected to ground around nMOS
  - N+ guard rings connected to V_{DD} around pMOS
- Place substrate and well contacts as close as possible to the source of MOS transistors
  - Reduce R_w and R_{sub}
- Minimum area p-wells (in case of twin-tub technology or n-type substrate)

Latch-Up Guidelines(2)

- Source diffusion regions of pMOS transistors should be placed.
  - Ensure the same potential between V_{DD} and p-wells
- In some n-well I/O circuits, wells can be eliminated by using only nMOS
- Avoid the forward biasing of source/drain junctions
  - Prevents injecting high current
- Lightly doped epitaxial layer on top of a heavily doped substrate
  - Shunts lateral currents from the vertical transistor
- Place nMOS close to V_{SS} and pMOS near V_{DD}
- Maintain sufficient space between pMOS and nMOS

I/O Cell Layout With Latch-Up Guidelines