Chapter 8
Sequential MOS Logic Circuits

S.M. Kang, Y. Leblebici, and C. Kim
Introduction (1)

- Sequential Circuit
- Classification of logic circuits

Combinational block + memory block

Based on behavior
Bistable Elements: Cross Coupled Inverter

- Static behavior of the two inverter basic bistable elements

\[ v_{o1} = v_{i2} \]
\[ v_{o2} = v_{i1} \]

VTC of the two inverters & qualitative view of the potential energy levels
Bistable Elements: Circuit

- Circuit diagram
- Time domain behavior

- Stable operating point: Two energy minima
- Unstable operating point: One energy maximum
  - All four transistors are in saturation
Bistable Elements: Small Signal (1)

- Small signal input and output currents of the inverters

\[
i_{g1} = i_{d2} = g_m v_{g2}, \quad i_{g2} = i_{d1} = g_m v_{g1} \quad (8.1)
\]

\[
v_{g1} = \frac{q_1}{C_g}, \quad v_{g2} = \frac{q_2}{C_g} \quad (8.2)
\]

\[
i_{g1} = C_g \frac{dv_{g1}}{dt}, \quad i_{g2} = C_g \frac{dv_{g2}}{dt} \quad (8.3)
\]

\[
(8.1) \Rightarrow (8.3)
\]

\[
g_m v_{g2} = C_g \frac{dv_{g1}}{dt}, \quad g_m v_{g1} = C_g \frac{dv_{g2}}{dt} \quad (8.2)
\]

\[
\frac{g_m}{C_g} q_1 = \frac{C_g}{g_m} \frac{d^2 q_1}{dt^2} \Rightarrow \frac{d^2 q_1}{dt^2} = \left(\frac{g_m}{C_g}\right)^2 q_1 \quad \Rightarrow \frac{d^2 q_1}{dt^2} = \frac{1}{\tau_0^2} q_1 \text{ with } \tau_0 = \frac{C_g}{g_m}
\]
Bistable Elements : Small Signal (2)

- The time domain solution

\[ q_1(t) = \frac{q_1(0) - \tau_0 q_1'(0)}{2} e^{-\frac{t}{\tau_0}} + \frac{q_1(0) - \tau_0 q_1'(0)}{2} e^{+\frac{t}{\tau_0}}, \quad q_1(0) = C_g v_{g1}(0) \]

\[ v_{o2}(t) = \frac{1}{2} (v_{o2}(0) - \tau_0 v_{o2}'(0)) e^{-\frac{t}{\tau_0}} + \frac{1}{2} (v_{o2}(0) + \tau_0 v_{o2}'(0)) e^{+\frac{t}{\tau_0}} \]

\[ v_{o1}(t) = \frac{1}{2} (v_{o1}(0) - \tau_0 v_{o1}'(0)) e^{-\frac{t}{\tau_0}} + \frac{1}{2} (v_{o1}(0) + \tau_0 v_{o1}'(0)) e^{+\frac{t}{\tau_0}} \]

\[ \therefore v_{g1} = v_{o2}, \quad v_{g2} = v_{o1} \]

- The time domain expressions (t is a large value)

\[ v_{o1}(t) \approx \frac{1}{2} (v_{o1}(0) + \tau_0 v_{o1}'(0)) e^{+\frac{t}{\tau_0}} \]

\[ v_{o2}(t) \approx \frac{1}{2} (v_{o2}(0) + \tau_0 v_{o2}'(0)) e^{+\frac{t}{\tau_0}} \]
Phase Plane Representation

- The bistable circuit behavior

\[ v_{o1} = V_{th}, \quad v_{o2} = V_{th} \]

Stable

\[ v_{o1} : V_{th} \rightarrow V_{OH} \quad \text{or} \quad V_{OL} \]

Unstable

\[ v_{o2} : V_{th} \rightarrow V_{OL} \quad \text{or} \quad V_{OH} \]
Propagation of a Transient Signal

- The time domain behavior:
  \[
  \frac{v_{o1}(t)}{v_{o1}(0)} = e^{\frac{t}{\tau_0}}
  \]

- The loop gain:
  \[
  A^n = e^{\frac{T}{\tau_0}}
  \]
SR Latch Circuit

- SR latch circuit based on NOR2 gates
- Gate level schematic and block diagram
Truth Table and Operation Mode

Truth table of the NOR based SR latch circuit

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>$Q_{n+1}$</th>
<th>$\overline{Q}_{n+1}$</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>$Q_n$</td>
<td>$\overline{Q}_n$</td>
<td>hold</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>set</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>reset</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>not allowed</td>
</tr>
</tbody>
</table>

Operation mode of the NOR based SR latch circuit

<table>
<thead>
<tr>
<th>$S$</th>
<th>$R$</th>
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</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>$V_{OL}$</td>
<td>$V_{OH}$</td>
<td>$V_{OL}$</td>
<td>M1 and M2 on, M3 and M4 off</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>$V_{OH}$</td>
<td>$V_{OL}$</td>
<td>$V_{OH}$</td>
<td>M1 and M2 off, M3 and M4 on</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OH}$</td>
<td>$V_{OL}$</td>
<td>M1 and M4 off, M2 on, or</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>$V_{OH}$</td>
<td>M1 and M4 off, M3 on</td>
</tr>
</tbody>
</table>
Circuit Diagram of the SR Latch

- Total lumped capacitance at each output node

\[ C_Q = C_{gb,2} + C_{gb,5} + C_{db,3} + C_{db,4} + C_{db,7} + C_{sb,7} + C_{db,8} \]

\[ C_{\overline{Q}} = C_{gb,3} + C_{gb,7} + C_{db,1} + C_{db,4} + C_{db,5} + C_{sb,5} + C_{db,6} \]

- Rise time:
  \[ \tau_{\text{rise},Q}(SR-latch) = \tau_{\text{rise},Q}(NOR2) + \tau_{\text{fall},\overline{Q}}(NOR2) \]
CMOS SR Latch: Another Type

- Pseudo nMOS SR latch circuit based on NOR2 gates
- SR latch based on NAND2 gates
NAND Based SR Latch

- Gate level schematic & Block diagram
- Pseudo-nMOS NAND-based SR latch circuit

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q_{n+1}</th>
<th>\overline{Q}_{n+1}</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>not allowed</td>
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<tr>
<td>0</td>
<td>1</td>
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<td>0</td>
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<td>1</td>
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<td>0</td>
<td>1</td>
<td>reset</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>\overline{Q}_n</td>
<td>\overline{Q}_n</td>
<td>hold</td>
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</tbody>
</table>
Clocked SR Latch

◆ Gate level schematic
◆ Input and output waveform

Level sensitive circuit
Clocked NOR Based SR Latch : AOI

- AOI-based implementation of the clocked NOR-based SR-latch Circuit

- very small transistor count
Clocked NAND-Based SR Latch Circuit

- Schematic w/ active low i/p (CK=S=0 for set or CK=R=0 for reset)

- Schematic w/ active high i/p (CK=S=1 for set or CK=R=1 for reset)
Clocked JK Latch

- Gate level schematic

- SR-latch: indeterminate when both inputs S and R are activated
- JK latch: adding two feedback lines from the outputs to the inputs
Clocked JK Latch : All NAND Implementation

- All-NAND implementation of the clocked JK latch circuit
Clocked JK Latch: Another Type

- Clocked NOR-based JK latch
- CMOS AOI JK latch
Clocked JK Latch : Truth Table

<table>
<thead>
<tr>
<th>$J$</th>
<th>$K$</th>
<th>$Q_n$</th>
<th>$\overline{Q}_n$</th>
<th>$S$</th>
<th>$R$</th>
<th>$Q_{n+1}$</th>
<th>$\overline{Q}_{n+1}$</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>hold</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
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<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>reset</td>
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<td></td>
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<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
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<td>1</td>
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<td>0</td>
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<td>1</td>
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<td>0</td>
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<td>toggle</td>
</tr>
<tr>
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<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>
Clocked JK Latch: Toggle Switch

- **Toggle Switch**
  - If both inputs are equal to logic 1, output will oscillate.
    (The clock pulse width < input to output propagation delay)
  - JK latch is operated exclusively in this mode
Master-Slave Flip-Flop

- Master-Slave Flip-Flop
  - Two cascaded stages are activated with opposite clock phases.
Master-Slave Flip-Flop: Operation

- Clock pulse \(\rightarrow 0\)
  - Master latch inactive (slave becomes active)

- Clock pulse \(\rightarrow 1\)
  - Slave latch inactive (master becomes active)

- No uncontrolled oscillation: \(J=K=1\)

- Ones catching problem
  - Unwanted o/p transition due to glitch at i/p
  - Sol.: edge-triggered
NOR Based Master-Slave Flip-Flop

- Circuit toggling when \( J=K=1 \)
  - one stage must be active at any given time → A NOR-Based master-slave flip-flop
Timing Diagram for (+)ve-edge Triggered FF
Data-Q & Clk-Q Delays
Timing Diagram for Latch
CMOS D-Latch

- Gate-level schematic
- Block diagram

- CK : 1 → Q assumes the value of the input D
- CK : 0 → Q preserve its state
CMOS D-Latch: Version 1

- Constructed by Two inverter loop + Two CMOS TG
- CK:1 $\rightarrow$ TG at input is activated
- CK:0 $\rightarrow$ TG at inverter loop is activated
CMOS D-Latch: Simplified version 1

- **Simplified schematic view and timing diagram**

- **Setup time & Hold time**
  - Setup time and hold time should be met
  - Any violation can cause metastability problems.
CMOS Master-Slave D-Latch: Version 2

- Constructed by simply cascading two D-latch circuits
  - First stage (Master): driven by CK signal
  - Second stage (Slave): driven by inverted CK signal
Master-Slave D-latch: Version2 Simulation

Simulated input and output waveforms of version 2

M-S Latch Transient Response

![Diagram showing the simulated waveforms for CK, CK_bar, D, Qm, and Qs over time (ns).]
Master-Slave D-latch: Setup Time Violation

Simulated waveforms master-slave D-latch circuit with setup time violation at 0.25ns
Master Slave D-Latch: Layout

Layout of the master-slave D-latch
C$^2$MOS Master-Slave D-Latch (Version 3)

- Constructed by four tri-state inverters
Pulsed Latch Based Clocked Storage Elements

- Advantages of HLFF: small D-Q delay, negative setup time, logic embedding with small penalty
- Minimum delay between FF should be guaranteed (due to increased hold time)

Semi Dynamic Flip-Flop (SDFF)

- SDFF to operate faster than HLFF
  - The back-end latch has only two stacked NMOS
- Disadvantage
  - Short pulse generators: Always toggle => large power consumption
EP-SFF Circuit

EP-SFF circuit and CK generator

- Advantages: Large amount of time borrowing, short output delay, energy and area efficient
- Disadvantage: Large hold time
Sense Amplifier Based Flip Flop (SAFF)

- Sensed amplifier based flip-flop circuit

- Disadvantage: Large propagation delay through SR latch
Modified SAFF

- To overcome large propagation delay of SAFF
- Cross-coupled Nand gates are replaced with a faster SR latch
Delay Comparison of CSE

- 0.13um CMOS technology with a supply voltage of 1.2V
Embedded Logic SDFF

<table>
<thead>
<tr>
<th></th>
<th>D</th>
<th>A•B</th>
<th>A+B</th>
<th>A•B+C•D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Embedded</td>
<td>199ps</td>
<td>219ps</td>
<td>229ps</td>
<td>246ps</td>
</tr>
<tr>
<td>Discrete</td>
<td>199ps</td>
<td>298ps</td>
<td>305ps</td>
<td>367ps</td>
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<tr>
<td>Speedup</td>
<td>1.0</td>
<td>1.36</td>
<td>1.33</td>
<td>1.49</td>
</tr>
</tbody>
</table>
Power Consumption Portion of Chips

- Adaptive Equalizer 1993: 35% Clk network only, 65% Rest of the Chip
- Microprocessor 1994: 18% Clk network only, 82% Rest of the Chip
- Microprocessor 1995: 40% Clk network only, 60% Rest of the Chip
- Microprocessor 2001: 70% Clk network only + FF, 30% Rest of the Chip
- Microprocessor 2005: 25% Clk network only, 75% Rest of the Chip
Power Consumption of Clocking

Power consumption of a particular clocking scheme

\[ P_{ck\text{-scheme}} = P_{ck\text{-network}} + P_{FF} \]

\[ P_{CK\text{-network}} = f_{CLK} \cdot \left\{ \left( C_{line} + C_{rep} + C_{ck\text{-tr}} \right) \cdot V_{ck\text{-swing}}^2 \right\} + V_{DD} \cdot I_{\text{leak,rep}} \]

(Dominated by dynamic power consumption)

Power dissipation by flip flops

\[ P_{FF} = \sum P_{ff} \]

\[ P_{ff} = \left\{ \left[ (\alpha_i C_i + \alpha_0 C_0) \cdot \beta + C_{local\text{-buf}} \cdot \gamma \right] \cdot V_{DD}^2 \right\} \cdot f_{CLK} + V_{DD} \cdot \left( I_{\text{leak,local\text{-buf}}} + I_{\text{leak,FF}} \right) \]

\( C_i \) : internal node Capacitance
\( \alpha_i \) : internal node transition ratio
\( C_{local\text{-buf}} \) : local clock buffer capacitance
\( \beta \) : 1 or 2 (for double-edge)
\( I_{\text{leak,local\text{-buf}}} \) : leakage current of local clock buffer
\( I_{\text{leak,FF}} \) : flip flop leakage current

\( C_0 \) : output node Capacitance
\( \alpha_0 \) : output node transition ratio
Low-Power CSEs

- Clock-on-demand FF
- Conditional capture FF
- Reduced swing clock FF
- Low-swing clock double-edge-triggered FF
Appendix: Schmitt Trigger

- Schmitt Trigger circuit

![Schmitt Trigger circuit diagram]
Schmitt Trigger : Positive Input Sweep (1)

1) \( V_{\text{in}} = 0V \)
   - M1, M2 : on
     \( V_x = V_y = V_{DD} = 1.2V \)
   - M3, M4, M5 : off
   - M6 : on (saturation), let \( V_{T,6} = 0.62V \)
     \( V_z = V_{DD} - V_{T,6} = 0.58V \)

2) \( V_{\text{in}} = V_{T0,n} = 0.48V \)
   - M5 : starts to turn on
   - M4 : off
     \( V_x = 1.2V \)
3) $V_{in} = 0.6V$

- M4 : off (assumption)
- M5, M6 : on (Saturation)

$$\frac{k_n}{2} \left( \frac{W}{L} \right)_5 \cdot \frac{E_C L_n}{(V_{in} - V_{T0,n}) + E_C L_n} = \frac{k_n}{2} \left( \frac{W}{L} \right)_6 \cdot \frac{E_C L_n}{(V_{DD} - V_z - V_{T,6}) + E_C L_n}$$

$$\Rightarrow \quad \frac{0.4 \cdot (0.6 - 0.48)^2}{(0.6 - 0.48) + 0.4} = \left( \frac{1}{10} \right) \cdot \frac{0.4 \cdot \left( 1.2 - V_z - \left[ 0.48 + 0.524(\sqrt{1.011 + V_z} - \sqrt{1.011}) \right] \right)^2}{1.2 - V_z - \left[ 0.48 + 0.524(\sqrt{1.011 + V_z} - \sqrt{1.011}) \right] + 0.4}$$

$$\Rightarrow \quad V_z = 0.18V$$

$$\Rightarrow \quad V_{GS,4} = 0.6 - 0.18 = 0.42 < V_{T0,n} = 0.48$$

M4 is indeed turned off
Schmitt Trigger: Positive Input Sweep (3)

4) $V_{in} = 0.62V$

- M5 : on (Linear), M6 : on (Saturation)
- $V_z$ is decreasing

$$\frac{k_n'}{2} \cdot \left(\frac{W}{L}\right)_5 \cdot \frac{1}{1 + \frac{V_z}{ECL_n}} \cdot \left[2 \cdot (V_{in} - V_{T0,n}) \cdot V_z - V_z^2\right] = \frac{k_n'}{2} \cdot \left(\frac{W}{L}\right)_6 \cdot \frac{ECL_n \cdot (V_{DD} - V_z - V_{T,6})^2}{(V_{DD} - V_z - V_{T,6}) + ECL_n \left(1 + \frac{V_z}{0.4}\right)} \cdot \left[2(0.62 - 0.48) \cdot V_z - V_z^2\right]$$

$$= \left(\frac{1}{10}\right) \cdot \left(1.2 - V_z - \left[0.48 + 0.524(\sqrt{1.011 + V_z} - \sqrt{1.011})\right]\right)^2$$

$$V_z = 0.1V$$

$V_{GS,4} = 0.62 - 0.1 = 0.52V > V_{T,n4} = 0.51$

- M4 : Already on
- $V_{th+} = 0.62V$ (Upper logic threshold voltage)
Schmitt Trigger: Negative Input Sweep (1)

1) $V_{in} = 1.2V$
   - M4, M5 : on $\Rightarrow V_X = 0V$
   - M1, M2 : off
   - M3 : on (Saturation)

\[
\frac{k_p'}{2} \cdot \left( \frac{W}{L} \right)_{3} \cdot \frac{E_c L_p \cdot (0 - V_y - V_{T,3})^2}{(0 - V_y - V_{T,3}) + E_c L_p} = 0
\]

\[
V_y = -V_{T,3} = - \left[ V_{T0, p} - 0.406 \left( \sqrt{0.972 + V_{DD}} - V_y - \sqrt{0.972} \right) \right]
\]

\[
V_y = 0.573V
\]

2) $V_{in} = 0.74V$
   - M1 : on
   - M2 : off
   - M3 : on (Saturation)
   - $V_{out}$ : unchanged
Schmitt Trigger: Negative Input Sweep (2)

3) $V_{\text{in}} = 0.6\text{V}$

- M1, M3: on (Saturation)

\[
\frac{k'_p}{2} \cdot \left( \frac{W}{L} \right) \cdot \frac{E_C L_p \cdot (V_{\text{in}} - V_{DD} - V_{T0,p})^2}{(V_{\text{in}} - V_{DD} - V_{T0,p}) + E_C L_p} = \frac{k'_p}{2} \cdot \left( \frac{W}{L} \right) \cdot \frac{E_C L_p \cdot (0 - V_y - V_{T3})^2}{(0 - V_y - V_{T3}) + E_C L_p} \cdot \frac{1.8 \cdot [0.6 - 1.2 - (-0.46)]^2}{[0.6 - 1.2 - (-0.46)] + 1.8}
\]

\[
1.8 \cdot [0.6 - 1.2 - (-0.46)]^2 
\]

\[
\frac{[0.6 - 1.2 - (-0.46)] + 1.8}{10} \cdot \frac{V_y = 0.92V \rightarrow V_{GS2} = 0.6 - 0.92 = -0.32 > V_{T0,p} = -0.46}{0 - V_y - \left[ -0.46 - 0.406(\sqrt{0.972 + 1.2 - V_y} - \sqrt{0.972}) \right] + 1.8}
\]

- M2: off (at this point)
Schmitt Trigger: Negative Input Sweep (3)

4) $V_{in} = 0.52V$
   - M2: off (Assumption)
   - M1: on (Linear), M3: on (Saturation)

$$\frac{k'_p \cdot \left( \frac{W}{L} \right)}{2} \cdot \frac{1}{1 + \frac{V_y}{E_{CL}}} \cdot \left[ 2 \cdot (V_{in} - V_{DD} - V_{T0,p}) \cdot (V_y - V_{DD}) - (V_y - V_{DD})^2 \right] = \frac{k'_p \cdot \left( \frac{W}{L} \right)}{2} \cdot \frac{E_{CL} \cdot (0 - V_y - V_{T3})}{(0 - V_y - V_{T3}) + E_{CL}}$$

$$\frac{1}{1 + \frac{V_y}{1.8}} \cdot [2 \cdot (0.52 - 1.2 - (-0.46)) \cdot (V_y - 1.2) - (V_y - 1.2)^2] = \left( \frac{1}{10} \right) \cdot 1.8 \cdot \left\{ 0 - V_y - \left[ -0.46 - 0.406 \left( \sqrt{0.972 + 1.2 - V_y - \sqrt{0.972}} \right) \right] \right\}$$

$\Rightarrow V_y = 0.98V$

$\Rightarrow$ M2 is already on
   - $V_{th-} = 0.52V$ (Lower logic threshold voltage)
Schmitt Trigger: Simulation

![Graph showing Schmitt Trigger output voltage vs input voltage. The graph illustrates two threshold voltages: $V_{th^-} = 0.51$ V for increasing input voltage, and $V_{th^+} = 0.63$ V for decreasing input voltage.](image)