

Solution

EE222 Midterm Examination

February 5, 2019

Name _____ Student ID _____

1. (10 points) In VLSI development estimation of required design effort in terms of engineer-months (EMs) is important. A handy empirical formula is shown below:

$EM = (1 + D)^{-yr} (A + B \cdot k^H)$, where k represents the number of equivalent transistors in the design expressed as

$$k = UNQ + C \cdot RPT + E \cdot PLA + F \cdot \sqrt{RAM} + G \cdot \sqrt{ROM}$$

in units of thousands (which means for 1M transistors in random access memory, RAM=1000) and A, B, C, D, E, F, G, and H are parameters that depend on the designers' experience and CAD tool support for the particular VLSI development .

Three years prior to the current project (thus $yr = 3$), the fitting parameters were

$$A=0, B=12, C= 0.15, D= 0.15, E = 0.1, F = 0.2, G = 0.1, \text{ and } H=1.2.$$

For a GPU development the estimated number of transistors are Random Access Memory- 3.6M transistors, Read Only Memory- 0.1M transistors, PLA transistors-0.4M transistors, Unique transistors- 0.1M transistors, Repeated transistors- 0.4M transistors

For the 20-engineer design team, estimate the numbers of months required for developing the GPU chip described above.

$$\begin{aligned} k &= 100 + 0.15(400) + 0.1(400) + 0.2(60) \\ &\quad + 0.1(10) = 213 \end{aligned}$$

$$EM = (1 + 0.15)^{-3} (0 + 12(213^{1.2})) = 4910.69$$

$$M (\text{Months}) = \frac{4910.69}{20} = 245.5 \text{ months}$$

The number of engineers (E) need to be increased ten-fold to finish the project in 2 yrs (24 months).

2. (20 points) For low power operation of CMOS circuits, describe the design principles in terms of speed requirement (delay specification), power supply voltages V_{DD} (multiple values), voltage swings ΔV at output nodes, switched capacitances C_{SW} (= product of switching frequency and capacitances), and MOS transistors' threshold voltages V_{th} (multiple values). For total power consumption, please include dynamic (switching) power, leakage power, and short circuit power.

$$P_{total} = \alpha C V_{DD} \Delta V f_{clock} + V_{DD} I_{leak} + V_{DD} I_{short}$$

To reduce power, "divide and conquer" approach would be effective, especially to take advantage of separating timing-critical paths and non-timing-critical paths. Also, at high level, turning power supply off (sleep mode) is highly effective. It reduces leakage power and of course dynamic power. But when the circuit is on, making use of $V_{th}(\text{low})$ transistors for timing critical paths while using $V_{th}(\text{high})$ transistors for non-timing critical paths is much desired to reduce power while meeting timing requirements. Since power is most influenced by V_{DD} and ΔV , reducing both while satisfying noise margins for signal integrity is highly effective.

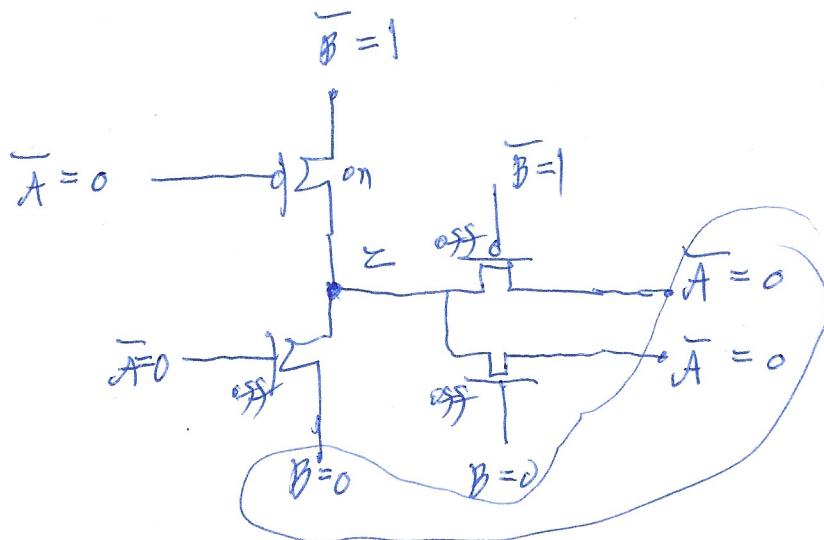
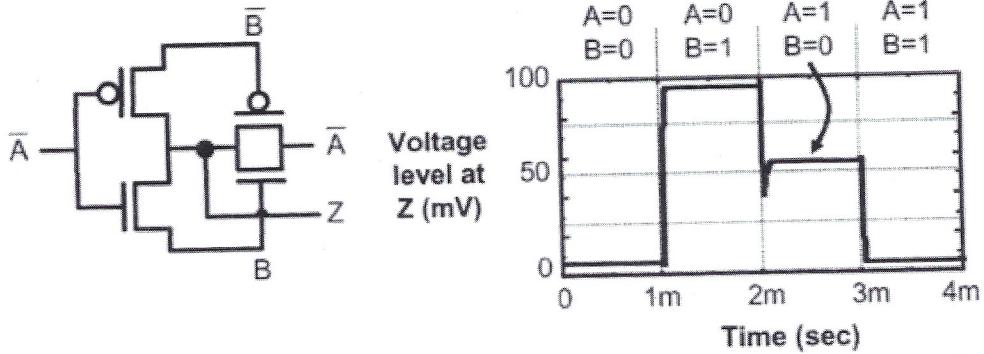
2. C needs to be reduced as much as possible by avoiding unnecessary switching and by achieving compact layout with minimal layout parasitics.

For leakage current reduction high V_{th} and low V_{DD} are desirable so long as delay requirements can be met.

To reduce/remove I_{short} , the input slew rates need to be high (\Rightarrow short rise/fall times in input signals of the gates). Low slew rates cause both PMOS and NMOS transistors turned on simultaneously, thus causing short circuits.

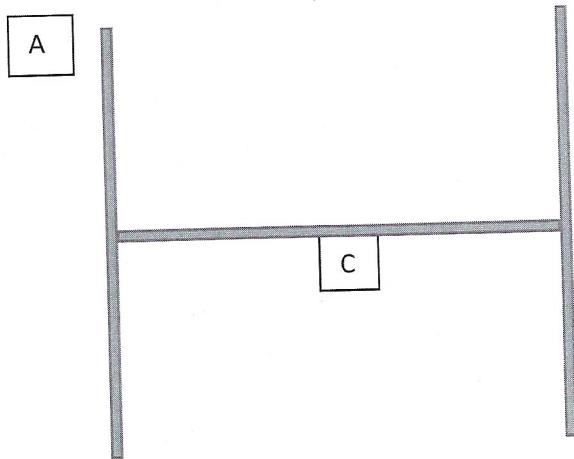
Also, multiple V_{DD} s can be used in order to reduce power with appropriate V_{DD} s and V_{th} values for different parts of the chip.

3. (20 points) Explain why the output voltage Z of an XOR gate is only about 50 mV for the time period of $2\text{mS} < t < 3\text{mS}$. What would cause this malfunction in this circuit?

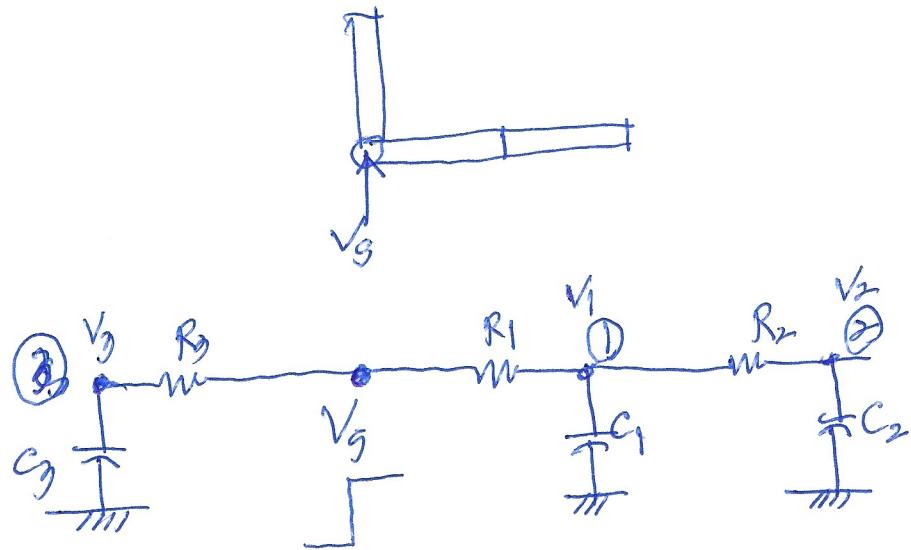


Although a single PMOS is turned on and tries to pull up node Z high, the three (1 PMOS, 2 NMOS) transistors' leakage currents pull down node Z . The time window (pulse width) of 1 ms is considered long enough to settle down the state (steady state).

4. (20 points) Let us consider an H-tree metal interconnect configuration of a uniform width $1 \mu\text{m}$ that distributes a clock signal from point C to four regions. Its horizontal length is $1000 \mu\text{m}$ and its vertical lengths are also $1000 \mu\text{m}$. Assuming that the line resistance is $0.05 \Omega/\text{square}$, and the effective line capacitance including the fringing field effect is $0.05 \text{ fF}/\mu\text{m}^2$, **find the Elmore delay from the center point C to the top left corner A.** For simple analysis use a distributed L-type RC model for every $250 \mu\text{m}$.



See the attachments



Nodal Analysis in S-domain

$$\text{Node 1} \quad (V_g - V_1) q_1 = V_1 C_1 s + q_2 (V_1 - V_2)$$

$$\text{Node 2} \quad q_2 (V_1 - V_2) = C_2 s V_2$$

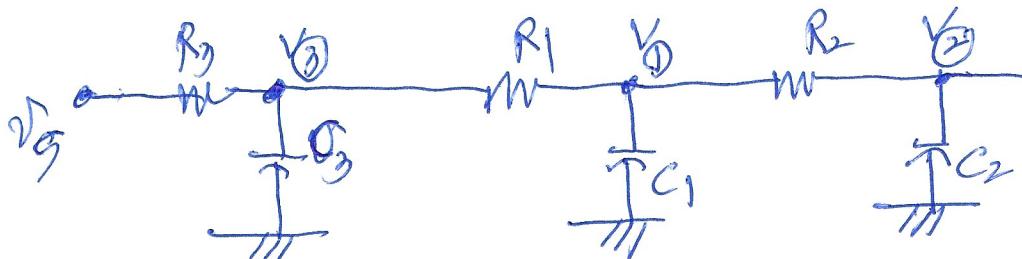
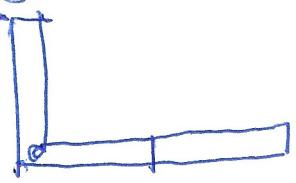
$$\text{Node 3} \quad C_3 s V_3 = q_3 (V_g - V_3)$$

$$\begin{bmatrix} (q_1 + q_2) + C_1 s & -q_2 & 0 \\ -q_1 & C_2 s + C_1 s & 0 \\ 0 & 0 & q_3 + C_3 s \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} q_1 V_g \\ -0 \\ q_3 V_g \end{bmatrix}$$

Note that Node 3 voltage is independent of Node 1, Node 2 voltages.

On the other hand, if the source voltage is located at node 3, then

$$V_3 \rightarrow$$



Nodal Analysis

$$\text{Node 3} \quad q_3(V_3 - V_3) = G_3 S V_3 + q_1(V_3 - V_1)$$

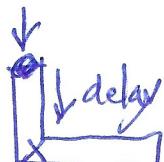
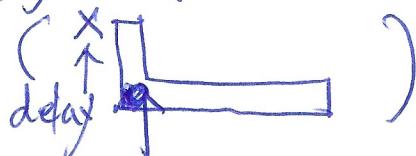
$$\text{Node 1} \quad q_1(V_3 - V_1) = G_1 S V_1 + q_2(V_1 - V_2)$$

$$\text{Node 2} \quad q_2(V_1 - V_2) = C_2 S V_2$$

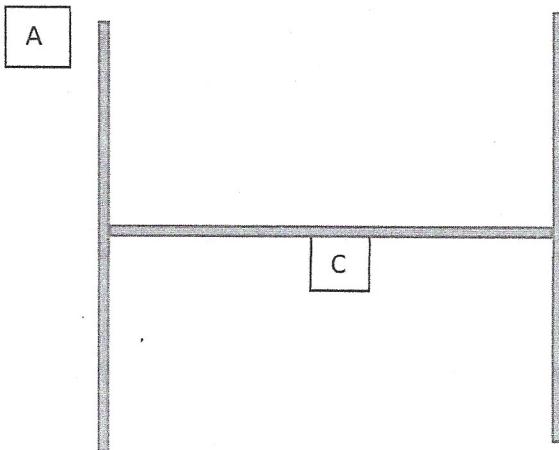
$$\begin{bmatrix} q_1 + q_2 + q_3 & -q_2 & -q_1 \\ -q_2 & q_2 + C_2 S & 0 \\ -q_1 & 0 & q_1 + q_2 + q_3 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ q_3 V_3 \end{bmatrix}$$

V_1, V_2, V_3 are all inter-related !

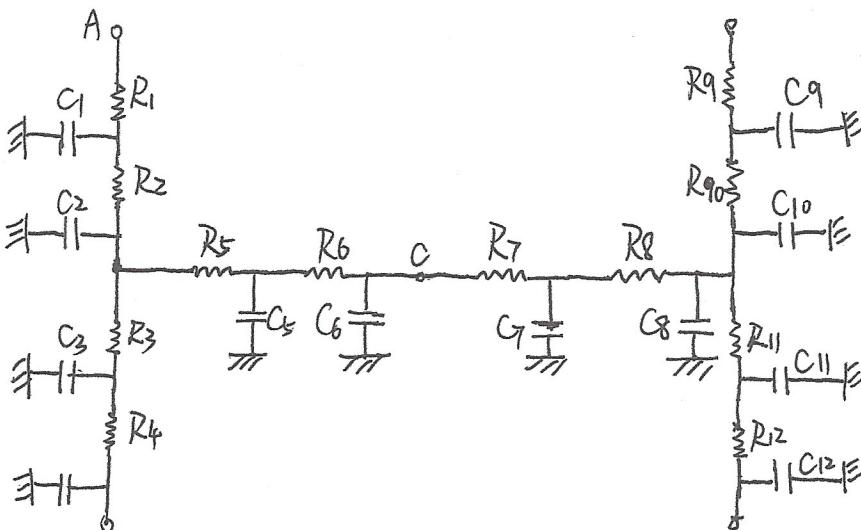
Thus driving the line from left end of
is different from driving the line in the middle.



4. (20 points) Let us consider an H-tree metal interconnect configuration of a uniform width 1 μm that distributes a clock signal from point C to four regions. Its horizontal length is 1000 μm and its vertical lengths are also 1000 μm . Assuming that the line resistance is 0.05 Ω/square , and the effective line capacitance including the fringing field effect is 0.05 fF/ μm^2 , find the Elmore delay from the center point C to the top left corner A. For simple analysis use a distributed L-type RC model for every 250 μm .



Solution:



Elmore delay ~~T_{AB}~~ T_{CA}

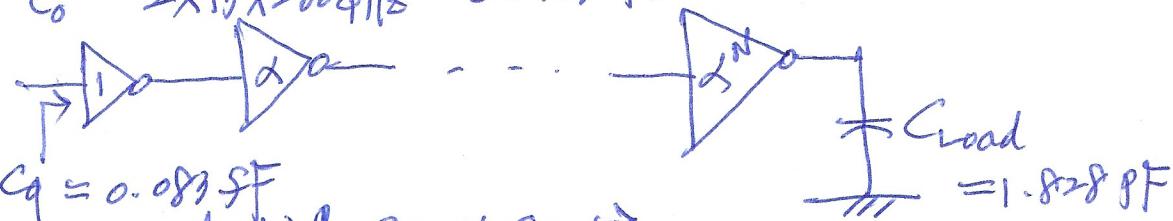
$$\begin{aligned}\cancel{T_{AB}} = T_{CA} &= R_6 C_6 + (R_5 + R_6) C_5 + (R_5 + R_6) C_3 + (R_5 + R_6) C_4 \\ &\quad + (R_5 + R_6 + R_2) C_2 + (R_5 + R_6 + R_1 + R_2) C_1\end{aligned}$$

$$R_0 = 0.05 \Omega/\square \times 250 \square = 12.5 \Omega \quad C_0 = 0.05 \text{ fF}/\mu\text{m}^2 \times 25.0 \mu\text{m}^2 = 12.5 \text{ fF}$$

$$\begin{aligned}T_{CA} &= R_0 C_0 (1 + 2 + 2 + 2 + 3 + 4) \\ &= 12.5 \times 12.5 \times 10^{-15} \times 14 \\ &= 2.19 \text{ ps}\end{aligned}$$

5. (30 points) A super buffer can be used to drive a large load capacitance C_{load} instead of abruptly enlarging the driving gate's transistor sizes. When the total input gate capacitance of an intrinsic inverter is $C_g = 0.083 \text{ fF}$ and $C_{load} = 1.828 \text{ pF}$, find the minimum delay achievable in picoseconds. It is known that the ring oscillator frequency is 200 GHz when 15 intrinsic inverters are cascaded. (Hint: The intrinsic inverter delay τ_0 can be found from the oscillation frequency. Also $C_{load}/C_g = e^{10}$ for $e = 2.718$.)

- $\tau_0 = \frac{1}{2 \times 15 \times 200 \text{ GHz}} = 0.167 \text{ ps}$



$$C_g = 0.083 \text{ fF}$$

neglecting $C_d \ll C_g \Rightarrow$

$$\omega^N = \frac{C_{load}}{C_g} = e \Rightarrow N \ln \omega = 10$$

- $N = \frac{10}{\ln \omega} = \frac{10}{\ln e} = 10$

$$\tau_{total} = N(\tau_0 \omega)$$

$$\frac{\partial \tau_{total}}{\partial \omega} = 0$$

$$\begin{aligned} \frac{\partial}{\partial \omega} [N \tau_0 \omega] &= \frac{\partial}{\partial \omega} \left[\frac{10}{\ln \omega} \tau_0 \omega \right] \\ &= 10 \tau_0 \frac{\partial}{\partial \omega} \left[\frac{\omega}{\ln \omega} \right] = 10 \tau_0 \left[\frac{\ln \omega - \omega \frac{1}{\omega}}{(\ln \omega)^2} \right] = 0 \end{aligned}$$

- $\boxed{\omega = e} *$

$$\begin{aligned} \tau_{total} &= N \tau_0 e = 10 \tau_0 e = 10(0.167 \text{ ps})(2.718) \\ &= \underline{4.54 \text{ ps}} \end{aligned}$$