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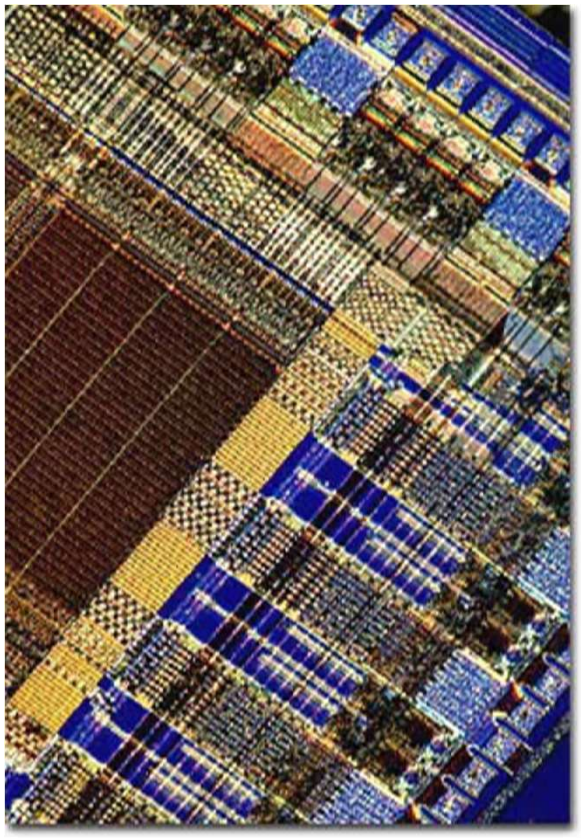
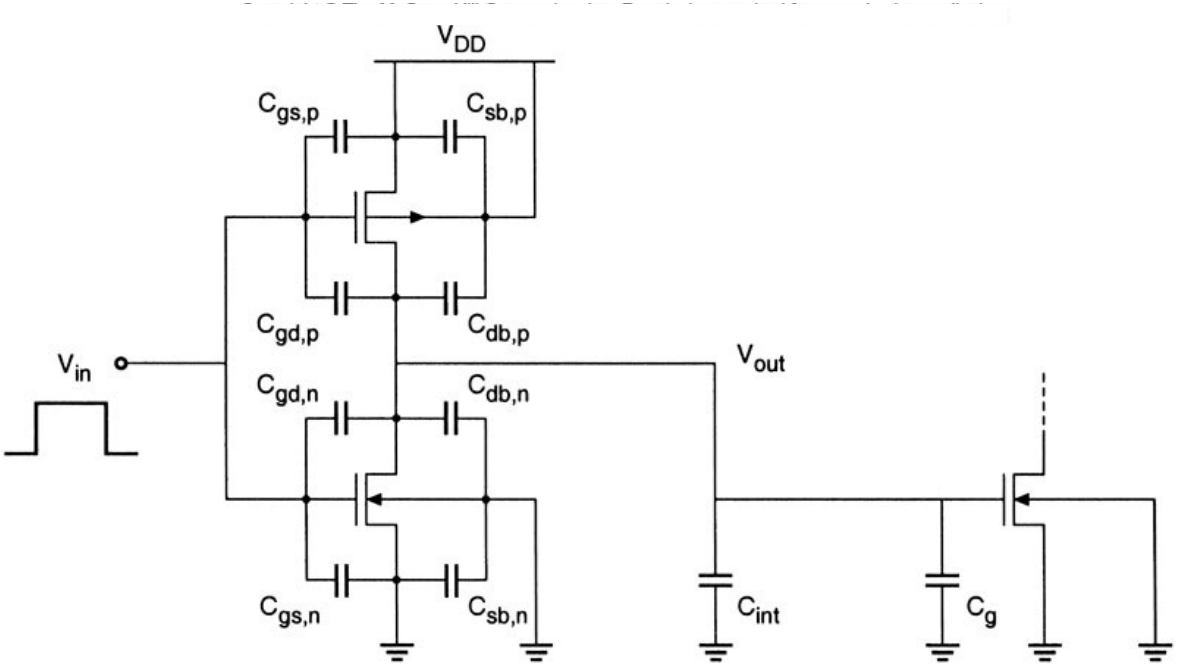


Chapter 6
MOS Inverters: Switching Characteristics and Interconnect Effects

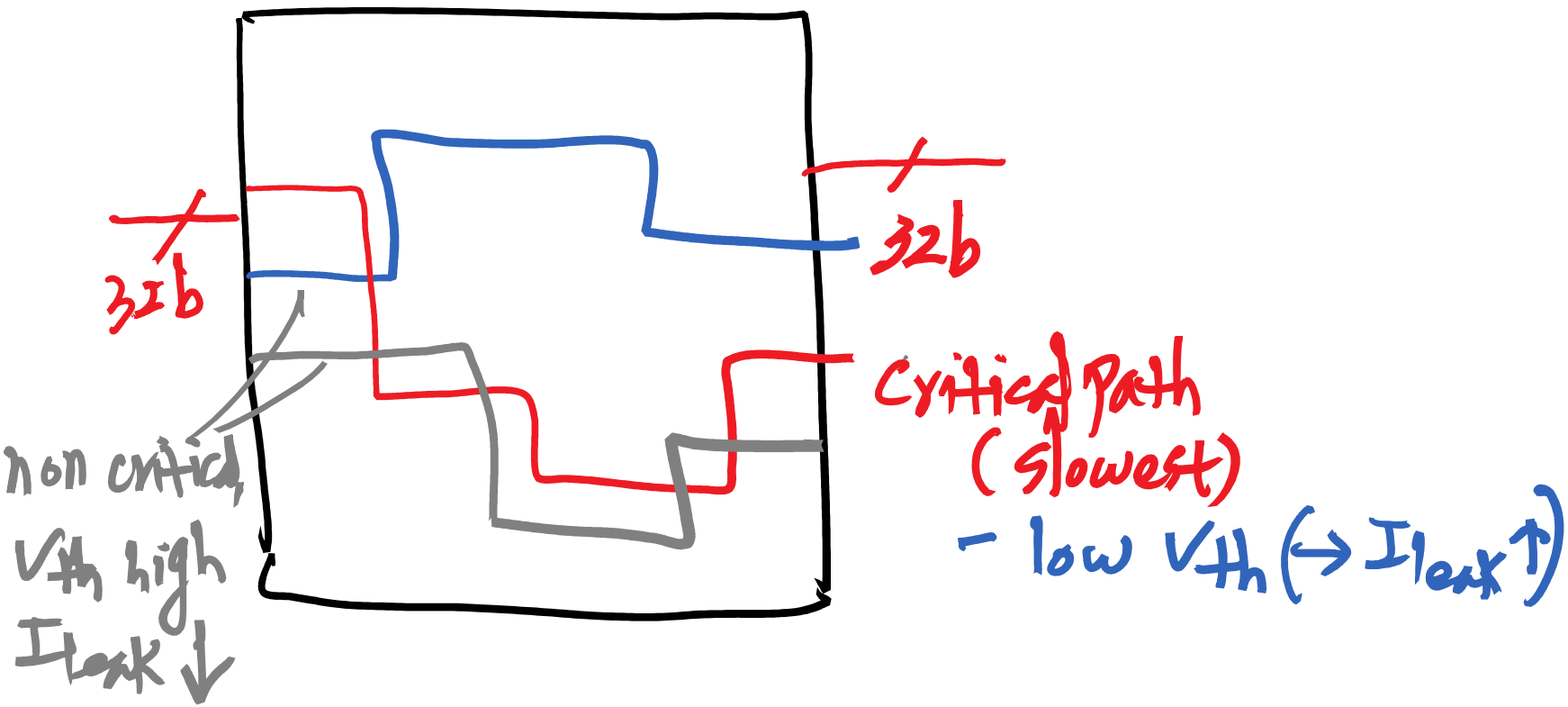
S.M. Kang, Y. Leblebici, and C. Kim

Introduction (1)

- Cascaded CMOS inverter stages

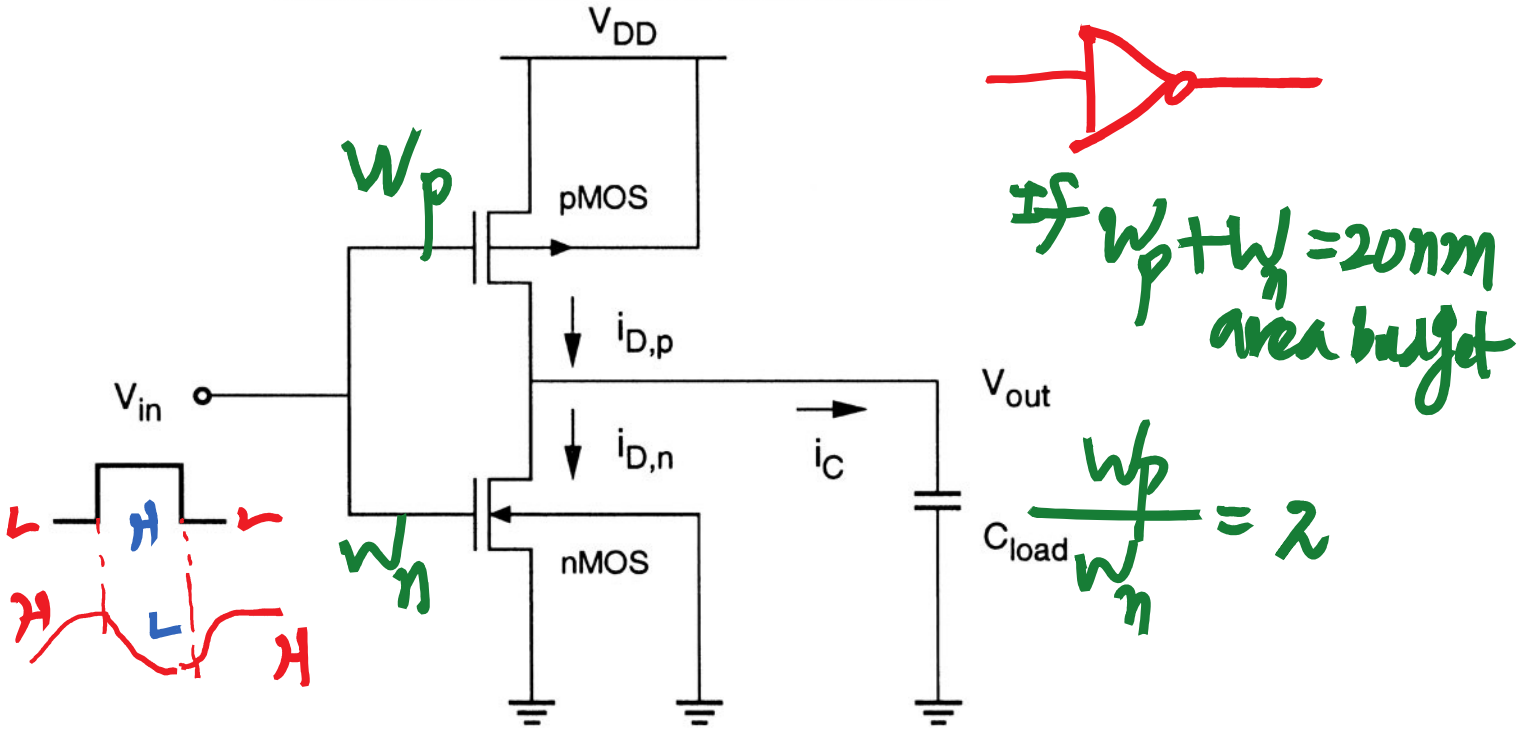


$$C_{load} = C_{gd,n} + C_{gd,p} + C_{db,n} + C_{db,p} + C_{int} + C_g$$



Introduction (2)

- First-stage CMOS inverter with lumped output load capacitance.



How to Choose an Optimal Ratio of Wp/Wn

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \approx 2$$

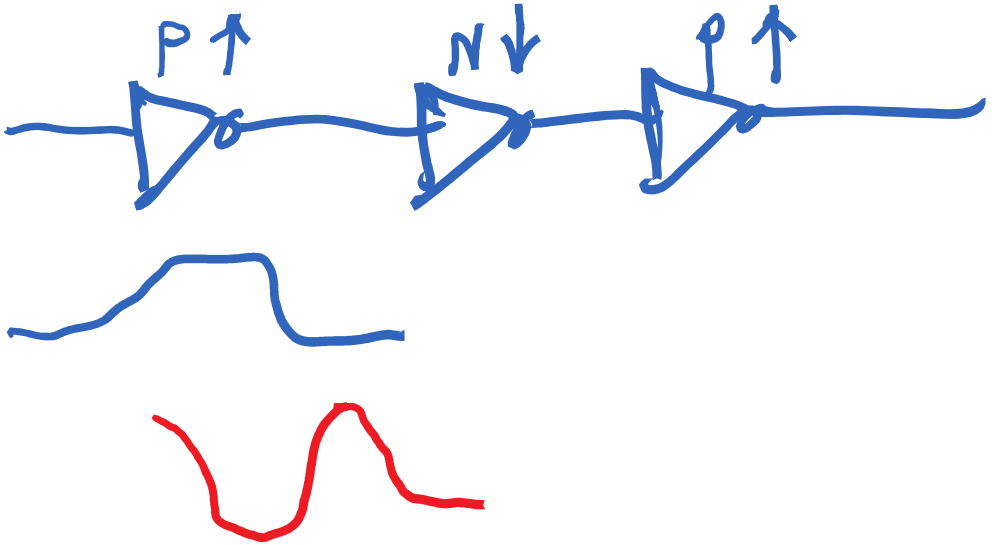
$$W_p = 2W_n$$

$$W_p + W_n = 2W_n + W_n = 20 \qquad W_n = \frac{20}{3} \approx 7\,nm$$

$$W_p = 13\,nm$$

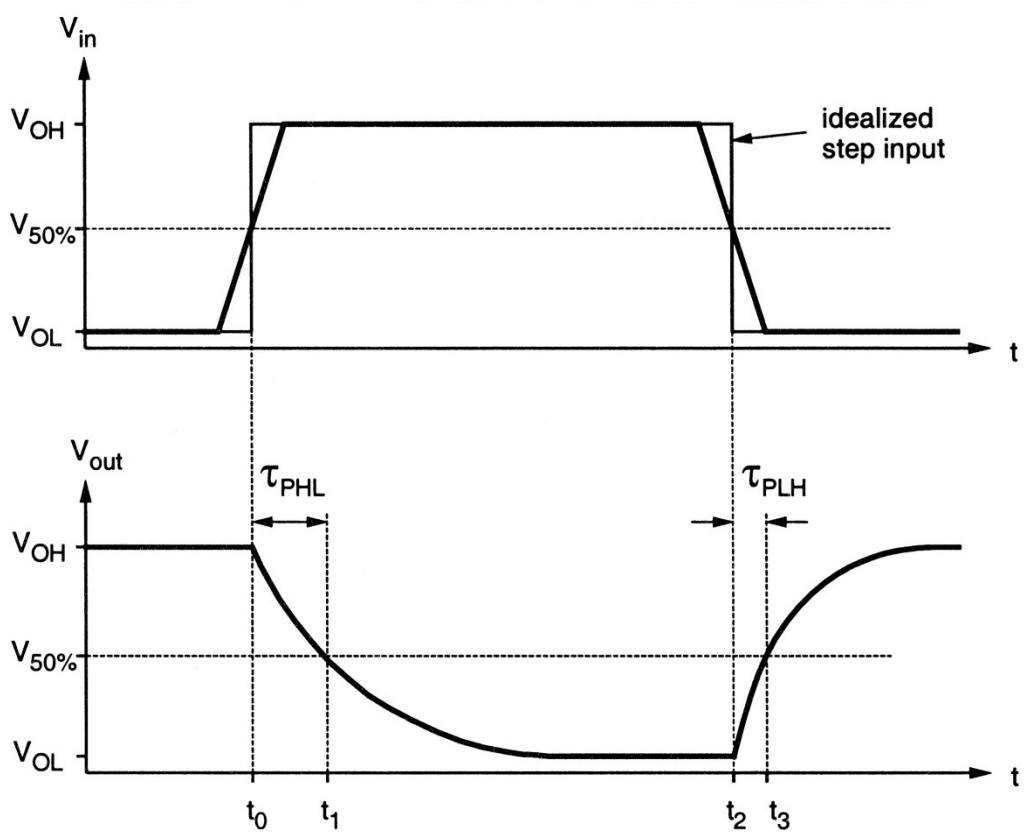
$$W_n = 10\,nm \qquad W_p = 10\,nm$$

Cascaded Connection of PMOS and NMOS in a Path



(Noise Margin consideration favors
$W_p/W_n = \mu_n/\mu_p$)

Delay-Time Definitions: Propagation Delays



$$V_{50\%} = V_{OL} + \frac{1}{2}(V_{OH} - V_{OL})$$

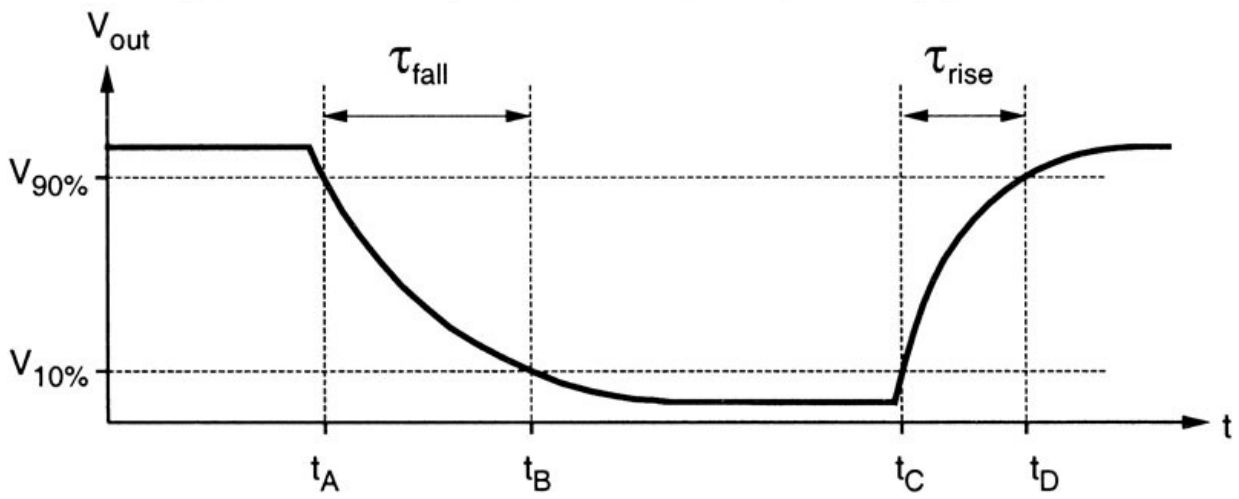
$$= \frac{1}{2}(V_{OL} + V_{OH})$$

$$\tau_{PHL} = t_1 - t_0$$

$$\tau_{PLH} = t_3 - t_2$$

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

Delay-Time Definitions: Rise & Fall Times



$$V_{10\%} = V_{OL} + 0.1 \cdot (V_{OH} - V_{OL})$$

$$V_{90\%} = V_{OL} + 0.9 \cdot (V_{OH} - V_{OL})$$

$$\tau_{fall} = t_B - t_A$$

$$\tau_{rise} = t_D - t_C$$

Calculation of Delay Times (1)

- Simplest method : estimating the average capacitance current

$$\tau_{PHL} = \frac{C_{load} \cdot \Delta V_{HL}}{I_{avg,HL}} = \frac{C_{load} \cdot \left(V_{OH} - V_{50\%}\right)}{I_{avg,HL}}$$

$$\tau_{PLH} = \frac{C_{load} \cdot \Delta V_{LH}}{I_{avg,LH}} = \frac{C_{load} \cdot \left(V_{50\%} - V_{OL}\right)}{I_{avg,LH}}$$

  - The average current

$$I_{avg,HL} = \frac{1}{2}\left[i_C\left(V_{in} = V_{OH}, V_{out} = V_{OH}\right) + i_C\left(V_{in} = V_{OH}, V_{out} = V_{50\%}\right)\right]$$

$$I_{avg,LH} = \frac{1}{2}\left[i_C\left(V_{in} = V_{OL}, V_{out} = V_{50\%}\right) + i_C\left(V_{in} = V_{OL}, V_{out} = V_{OL}\right)\right]$$

Calculation of Delay Times (2)

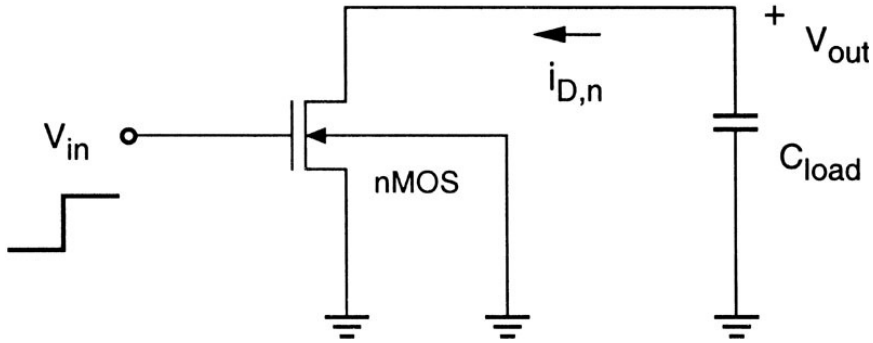
- More accurate method: solving the state equation of the output node in time domain
  - The capacitance current

$$C_{load}\frac{dV_{out}}{dt} = i_C = i_{D,p} - i_{D,n}$$

  - The rising-input case

$$i_{D,p} \approx 0$$

$$C_{load}\frac{dV_{out}}{dt} = i_C = -i_{D,n}$$



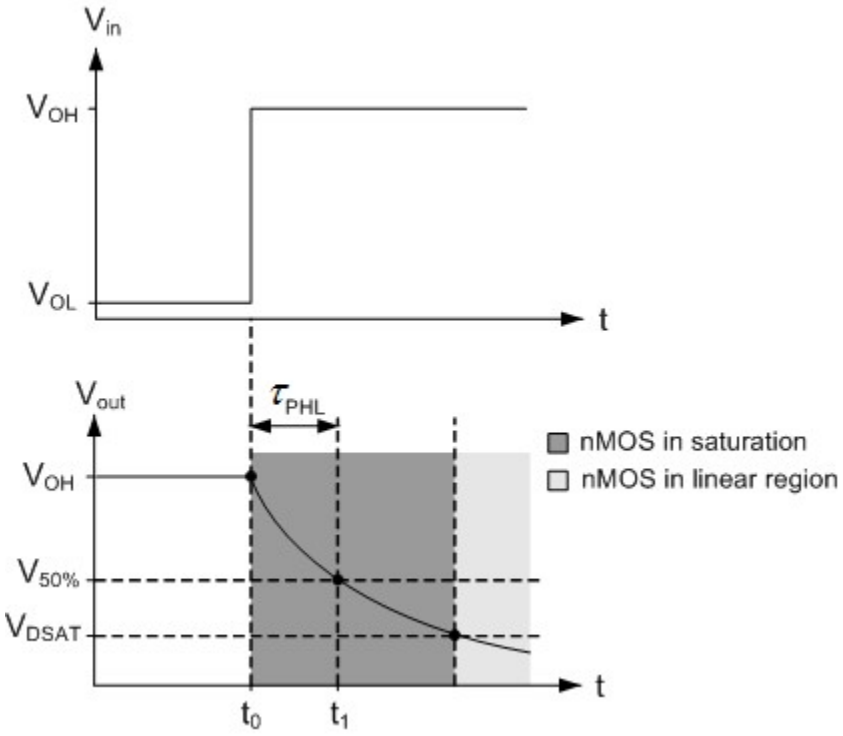
Calculation of Delay Times (3)

- Calculation of the propagation delay time

$$i_{D,n} = W \cdot v_{sat} \cdot C_{ox} \cdot \frac{(V_{in} - V_{T,n})^2}{(V_{in} - V_{T,n}) + E_C L}$$

$$= W \cdot v_{sat} \cdot C_{ox} \cdot \frac{(V_{OH} - V_{T,n})^2}{(V_{OH} - V_{T,n}) + E_C L},$$

$$for \quad V_{DSAT} < V_{out} \leq V_{OH}$$



Calculation of Delay Times (4)

$$\int_{t=t_0}^{t=t_1} dt = -C_{load}\int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{50\%}} \left(\frac{1}{i_{D,n}}\right) dV_{out} = -\frac{\left[\left(V_{OH}-V_{T,n}\right)+E_C L\right]C_{load}}{W v_{sat} C_{ox}\left(V_{OH}-V_{T,n}\right)^2}\int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{50\%}} dV_{out}$$

$$t_1 - t_0 = \frac{\left[\left(V_{OH}-V_{T,n}\right)+E_C L\right]C_{load}V_{50\%}}{W v_{sat} C_{ox}\left(V_{OH}-V_{T,n}\right)^2}$$

- The propagation delay time for high-to-low output transition

$$\tau_{PHL} = \frac{C_{load}}{k_n}\cdot\frac{2}{E_C L}\cdot\frac{V_{50\%}\left[\left(V_{OH}-V_{T,n}\right)+E_C L\right]}{\left(V_{OH}-V_{T,n}\right)^2}$$

- For $V_{OH}=V_{DD}$ and $V_{OL}=0$,

$$\tau_{PHL} = \frac{C_{load}}{k_n}\cdot\frac{2}{E_C L}\cdot\frac{V_{50\%}\left[\left(V_{DD}-V_{T,n}\right)+E_C L\right]}{\left(V_{DD}-V_{T,n}\right)^2}$$

Example 6.1 (1)

- Calculate the delay time of CMOS inverter necessary for the output to fall from its initial value of 1.2V to 0.6V
  - V_{DD}=1.2V, I_{SAT}=2mA for $V_{DS} \geq 0.27V$
  - output load capacitance of 30fF

- Sol.
  - From t=0 to $t=t_1=t_{delay}$ (saturation region)
  - For the saturation region

$$C\frac{dV_{out}}{dt} = -I_D = -I_{sat} = -W \cdot v_{sat} \cdot C_{ox} \cdot \frac{(V_{OH} - V_{T,n})^2}{(V_{OH} - V_{T,n}) + E_C L_n}$$

Example 6.1 (2)

- The amount of time in which the nMOS transistor operates in saturation

$$\int_{t=0}^{t=t_{delay}} dt = -\int_{V_{out}=1.2}^{V_{out}=0.6} \frac{C}{I_D} dV_{out}$$

- The total delay time

$$t_{delay} = \frac{\Delta V \cdot C}{I_{sat}} = \frac{0.6V \times 30\,fF}{2mA} = 9\ [ps]$$

Example 6.2 (1)

- Determine τ_{fall} ($V_{90\%}$~$V_{10\%}$) of CMOS inverter using both the average-current method and the differential equation method
  - V_{DD}=1.2V
  - $\mu_n C_{ox}$=0.983mA/V^2, $(W/L)_n$=10, $V_{T,n}$=0.53V, $E_{c,n}L_n$ = 0.45
  - An output load capacitance of 30fF
- Sol.
  - 1) Using the weighted average-current method: average capacitor current

$$I_{avg} = \frac{V_{90\%} - V_{ds,sat}}{\Delta V} I(V_{in} = 1.2V, V_{out} = 1.08V) + \frac{V_{ds,sat} - V_{10\%}}{\Delta V} I(V_{in} = 1.2V, V_{out} = 0.12V)$$

$$= \frac{V_{90\%} - V_{ds,sat}}{V_{90\%} - V_{10\%}} \cdot W \cdot v_{sat} \cdot C_{ox} \cdot \frac{(V_{in} - V_{T,n})^2}{(V_{in} - V_{T,n}) + E_C L} + \frac{V_{ds,sat} - V_{10\%}}{V_{90\%} - V_{10\%}} \cdot \frac{k_n}{2} \frac{1}{\left(1 + \frac{V_{out}}{E_C L_n}\right)} \left[2 \cdot (V_{in} - V_{T,n}) \cdot V_{out} - V_{out}^2\right]$$

Example 6.2 (2)

$$= \frac{1.08-0.27}{0.96} \cdot \frac{0.983\times10^{-3}\times0.45\times10}{2} \cdot \frac{(1.2-0.53)^2}{(1.2-0.53)+0.45}$$

$$+ \frac{0.27-0.12}{0.96} \cdot \frac{0.983\times10^{-3}\times10}{2} \cdot \frac{1}{\left(1+\frac{0.12}{0.45}\right)}\left[2\times(1.2-0.53)\times0.12-0.12^2\right]$$

$$= 0.84[mA]$$

- The fall time

$$\tau_{fall} = \frac{C\cdot\Delta V}{I_{avg}} = \frac{30\times10^{-15}\times0.96}{0.84\times10^{-3}} = 34.2[ps]$$

Example 6.2 (3)

- 2) Using the differential equation approach
- The current equation for saturation region

$$C\frac{dV_{out}}{dt} = -W \cdot v_{sat} \cdot C_{ox} \cdot \frac{(V_{in} - V_{T,n})^2}{(V_{in} - V_{T,n}) + E_C L}$$

$$\frac{dV_{out}}{dt} = -\frac{0.983\times10^{-3}\times10\times0.45}{2\times30\times10^{-15}} \cdot \frac{(1.2-0.53)^2}{(1.2-0.53)+0.45} = -2.95\times10^{10}$$

- The time during which the nMOS operates in saturation

$$\int_{t=0}^{t=t_{sat}} dt = -\frac{1}{2.95\times10^{10}} \int_{V_{out}=1.08}^{V_{out}=0.27} dV_{out}$$

$$t_{sat} = \frac{0.81}{2.95\times10^{10}} = 27.5\ [ps]$$

Example 6.2 (4)

- The current equation for linear region

$$C\frac{dV_{out}}{dt} = -\frac{k_n}{2}\frac{1}{\left(1+\frac{V_{out}}{E_C L_n}\right)}\left[2\cdot(V_{in}-V_{T,n})\cdot V_{out}-{V_{out}}^2\right]$$

$$\int_{t=t_{sat}}^{t=t_{delay}} dt = -2C_{load}\int_{V_{out}=0.27}^{V_{out}=0.12}\left\{\frac{1+\frac{1}{E_C L}V_{out}}{k_n\left[2\left(V_{OH}-V_{T,n}\right)V_{out}-{V_{out}}^2\right]}\right\}dV_{out}$$

$$\tau_{fall}-t_{sat} = \frac{30\times10^{-15}}{9.83\times10^{-3}}\left[\frac{1}{(1.2-0.53)}\ln\left(\frac{4\left(2\left(1.2-0.53\right)-0.12\right)}{2\left(1.2-0.53\right)-0.27}\right)\right.$$

$$\left.+\frac{2}{0.45}\ln\left(\frac{2\left(1.2-0.53\right)-0.12}{2\left(1.2-0.53\right)-0.27}\right)\right] = 8.7\ [ps]$$

- Total fall time

$$\tau_{fall} = 27.5+8.7 = 36.2[ps]$$

The Propagation Delay Time

- Propagation delay time for low to high transition

$$\tau_{PLH} = \frac{C_{load}}{k_p} \cdot \frac{2}{E_C L} \cdot \frac{V_{50\%}\left(V_{OH} - V_{OL} - \left|V_{T,p}\right| + E_C L\right)}{\left(V_{OH} - V_{OL} - \left|V_{T,p}\right|\right)^2}$$

- For $V_{OH}=V_{DD}$, $V_{OL}=0$,

$$\tau_{PLH} = \frac{C_{load}}{k_p} \cdot \frac{2}{E_C L} \cdot \frac{V_{50\%}\left(V_{DD} - \left|V_{T,p}\right| + E_C L\right)}{\left(V_{DD} - \left|V_{T,p}\right|\right)^2}$$

- The sufficient conditions for *balanced* propagation delays, i.e., for $\tau_{PHL} = \tau_{PLH}$

$$V_{T,n} = \left|V_{T,p}\right| \quad \text{and}$$

$$E_{c,n} k_n = E_{c,p} k_p \ \left(\text{or } W_p / W_n = E_{c,n}\mu_n / E_{c,p}\mu_p\right)$$

Propagation Delay Time w/ Finite τ_r & τ_f

- Empirical equations

$$\tau_{PHL}(actual) = \sqrt{\tau_{PHL}^2(step\ input) + \left(\frac{\tau_r}{2}\right)^2}$$

$$\tau_{PLH}(actual) = \sqrt{\tau_{PLH}^2(step\ input) + \left(\frac{\tau_f}{2}\right)^2}$$

Inverter Design with Delay Constraints

- Given a required delay value, the (W/L)-ratio of the nMOS :

$$\left(\frac{W_n}{L_n}\right)=\frac{C_{load}}{\tau^*_{PHL}\mu_n C_{ox}}\cdot\frac{2}{E_C L_n}\cdot\frac{V_{50\%}\left[\left(V_{OH}-V_{T,n}\right)+E_C L_n\right]}{\left(V_{OH}-V_{T,n}\right)^2}$$

- Given a required delay value, the (W/L)-ratio of the pMOS :

$$\left(\frac{W_p}{L_p}\right)=\frac{C_{load}}{\tau^*_{PLH}\mu_p C_{ox}}\cdot\frac{2}{E_C L_p}\cdot\frac{V_{50\%}\left(V_{OH}-V_{OL}-\left|V_{T,p}\right|+E_C L_p\right)}{\left(V_{OH}-V_{OL}-\left|V_{T,p}\right|\right)^2}$$

Example 6.3 (1)

- Design a CMOS inverter (determine W_n and W_p) to meet the following specifications.
  - V_{th}=0.6V for V_{DD}=1.2V
  - $\tau_{PHL}^{*} \leq 20$ps, $\tau_{PLH}^{*} \leq 15$ps
  - A falling delay of 40ps for an output transition from 0.8V to 0.1V
  - A combined output load capacitance of 10fF

  - $\mu_n C_{ox}$=184 μA/V^2, $V_{T0,n}$=0.5V, $E_{c,n}L_n$ = 0.3
  - $\mu_p C_{ox}$=46 μA/V^2, $V_{T0,p}$=-0.48V, $E_{c,p}L_p$ = 1.2
  - L=40nm, W_{min}=300nm

Example 6.3 (2)

- Sol.
  - The minimum (W/L) ratio of nMOS

$$\left(\frac{W_n}{L_n}\right)=\frac{C_{load}}{\tau^*_{PHL}\mu_n C_{ox}}\cdot\frac{2}{E_C L}\cdot\frac{V_{50\%}\left(V_{DD}-V_{T,n}+E_C L\right)}{\left(V_{DD}-V_{T,n}\right)^2}$$

$$=\frac{10\times10^{-15}}{20\times10^{-12}\times184\times10^{-6}}\cdot\frac{2}{0.3}\cdot\frac{0.6\left(1.2-0.5+0.3\right)}{\left(1.2-0.5\right)^2}$$

$$=22$$

  - The minimum (W/L) ratio of pMOS

$$\left(\frac{W_p}{L_p}\right)=\frac{C_{load}}{\tau^*_{PLH}\mu_p C_{ox}}\cdot\frac{2}{E_C L}\cdot\frac{V_{50\%}\left(V_{DD}-\left|V_{T,p}\right|+E_C L\right)}{\left(V_{DD}-\left|V_{T,p}\right|\right)^2}$$

$$=\frac{10\times10^{-15}}{15\times10^{-12}\times46\times10^{-6}}\frac{2}{1.2}\frac{0.6\left(1.2-0.48+1.2\right)}{\left(1.2-0.48\right)^2}$$

$$=53.4$$

Example 6.3 (3)

$$V_{D,sat,n} = \frac{\left(V_{in} - V_{T,n}\right) \cdot E_C L_n}{\left(V_{in} - V_{T,n}\right) + E_C L_n} = \frac{\left(1.2 - 0.5\right) \times 0.3}{\left(1.2 - 0.5\right) + 0.3} = 0.21V$$

$$C_{load} \frac{dV_{out}}{dt} = -\frac{k_n}{2} \frac{\left(V_{in} - V_{T,n}\right)^2 \cdot E_C L_n}{\left(V_{in} - V_{T,n}\right) + E_C L_n} \qquad V_{out} \geq 0.21V$$

$$C_{load} \frac{dV_{out}}{dt} = -\frac{k_n}{2} \frac{1}{\left(1 + \frac{V_{out}}{E_C L_n}\right)} \left[2 \cdot (V_{in} - V_{T,n}) \cdot V_{out} - {V_{out}}^2\right] \qquad V_{out} < 0.21V$$

$$t_{delay} = 40 \times 10^{-12} = -2C_{load} \int_{V_{out}=0.8}^{V_{out}=0.21} \left\{ \frac{\left(V_{in} - V_{T,n}\right) + E_C L_n}{k_n \cdot \left(V_{in} - V_{T,n}\right)^2 \cdot E_C L_n} \right\} dV_{out}$$

$$-2C_{load} \int_{V_{out}=0.21}^{V_{out}=0.1} \left\{ \frac{1 + \frac{1}{E_C L} V_{out}}{\mu_n C_{ox} \left(\frac{W_n}{L_n}\right) \left[2\left(V_{OH} - V_{T,n}\right) V_{out} - {V_{out}}^2\right]} \right\} dV_{out}$$

Example 6.3 (4)

$$t_{delay} = -2C_{load} \cdot \frac{1}{\mu_n C_{ox}\left(\frac{W_n}{L_n}\right)} \cdot \frac{\left(V_{in} - V_{T,n}\right) + E_C L_n}{\left(V_{in} - V_{T,n}\right)^2 \cdot E_C L_n} \cdot \int_{V_{out}=0.8}^{V_{out}=0.21} dV_{out}$$

$$-2C_{load} \cdot \frac{1}{\mu_n C_{ox}\left(\frac{W_n}{L_n}\right)} \cdot \int_{V_{out}=0.21}^{V_{out}=0.1} \left\{ \frac{1 + \frac{1}{E_C L} V_{out}}{\left[2\left(V_{OH} - V_{T,n}\right)V_{out} - V_{out}^{\,2}\right]} \right\} dV_{out}$$

$$t_{delay} = -2 \times \frac{10 \times 10^{-15}}{184 \times 10^{-6} \times \left(\frac{W_n}{L_n}\right)} \times \frac{\left(1.2 - 0.5\right) + 0.3}{\left(1.2 - 0.5\right)^2 \times 0.3} \times (-0.59)$$

$$-2 \times \frac{10 \times 10^{-15}}{184 \times 10^{-6} \times \left(\frac{W_n}{L_n}\right)} \times \ln\frac{0.1}{0.21} \times \left(\frac{1}{1.4} + \frac{1.7}{0.42}\right)$$

$$40 \times 10^{-12} = \frac{10 \times 10^{-15}}{184 \times 10^{-6}\left(\frac{W_n}{L_n}\right)} \left[4.01 + 3.53\right]$$

$$\left(\frac{W_n}{L_n}\right) = 10.24$$

Example 6.3 (5)

- The logic threshold voltage of the CMOS inverter,

$$V_{th} = \frac{V_{T0,n} + \sqrt{\kappa} \cdot \left(V_{DD} - \left| V_{T0,p} \right| \right)}{1 + \sqrt{\kappa}} = 0.6 \qquad \kappa = \frac{W_p}{W_n} \cdot \frac{E_{C,n} \cdot L_n}{E_{C,p} \cdot L_p}$$

$$\kappa = \frac{\left(\frac{W_p}{L_p} \right)}{\left(\frac{W_n}{L_n} \right)} \cdot \frac{E_{C,n}}{E_{C,p}} = \frac{\left(\frac{W_p}{L_p} \right) \times 0.3}{3.9 \times 1.2} = 0.694 \qquad \left(\frac{W_p}{L_p} \right) = 61.1$$

- Determine nMOS : W_n=880nm, L_n=40nm
- Determine pMOS : W_p=2,440nm, L_p=40nm

A Design of CMOS Polycells (Standard Cells)

IEEE Trans. On Circuits and Systems, vol. CAS-28, no. 8, Aug. 1981.

(abstract)- this was for 2.5 um CMOS technology

A Design of CMOS Polycells for LSI Circuits

SUNG MO KANG

Abstract— We have designed CMOS polycells with a uniform height for LSI random logic circuits. The design objective was to minimize the product of propagation delay and chip area while allowing noise margins to be at least 25 percent of V_{dd}. Designable parameters were identified to be channel widths in p-type and n-type transistors. Analytical models were derived to show the existence of an optimal solution point. Physical interpretations of models were also given. SPICE was used to simulate propagation delays and noise margins in inverter (INR), 2- and 3-input NAND and NOR gates under worst-case conditions. The chip performance of polycell-based CMOS circuits was then estimated by averaging performances of these five logic gates. With 3.5-μm design rules, the channel widths in p-channel and n-channel transistors were designed to be 35 μm and 17 μm, respectively.

Output Load Capacitance

$$C_{load} = C_{gd,n}(W_n) + C_{gd,p}(W_p) + C_{db,n}(W_n) + C_{db,p}(W_p) + C_{int} + C_g$$
$$= f(W_n, W_p)$$

$$C_{db,n} = W_n D_{drain} C_{j0,n} K_{eq,n} + 2(W_n + D_{drain}) C_{jsw,n} K_{eq,n}$$

$$C_{db,p} = W_p D_{drain} C_{j0,p} K_{eq,p} + 2(W_p + D_{drain}) C_{jsw,p} K_{eq,p}$$

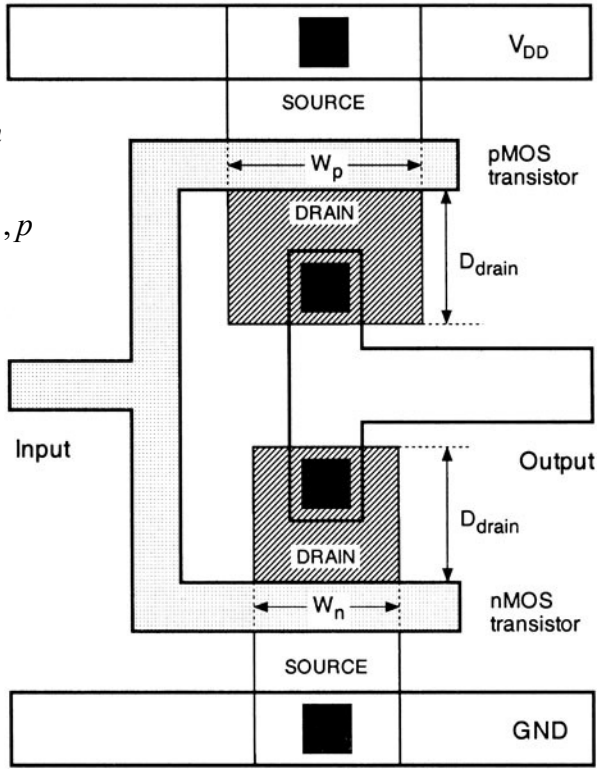
$$C_{load} = \alpha_0 + \alpha_n W_n + \alpha_p W_p$$

where

$$\alpha_0 = 2D_{drain}(C_{jsw,n} K_{eq,n} + C_{jsw,p} K_{eq,p}) + C_{int} + C_g$$

$$\alpha_n = K_{eq,n}(C_{j0,n} D_{drain} + 2C_{jsw,n})$$

$$\alpha_p = K_{eq,p}(C_{j0,p} D_{drain} + 2C_{jsw,p})$$



The Propagation Delay Expressions

$$\tau_{PHL} = \left(\frac{\alpha_0 + \alpha_n W_n + \alpha_p W_p}{W_n}\right) \cdot \left(\frac{L_n}{\mu_n C_{ox}}\right) \cdot \frac{2}{E_{C,n} L_n} \cdot \frac{V_{50\%}\left[\left(V_{DD} - V_{T,n}\right) + E_{C,n} L_n\right]}{\left(V_{DD} - V_{T,n}\right)^2}$$

$$\tau_{PLH} = \left(\frac{\alpha_0 + \alpha_n W_n + \alpha_p W_p}{W_p}\right) \cdot \left(\frac{L_p}{\mu_p C_{ox}}\right) \cdot \frac{2}{E_{C,p} L_p} \cdot \frac{V_{50\%}\left(V_{DD} - \left|V_{T,p}\right| + E_{C,p} L_p\right)}{\left(V_{DD} - \left|V_{T,p}\right|\right)^2}$$

$$R \equiv \left(\frac{W_p}{W_n}\right) \longrightarrow \tau_{PHL} = \Gamma_n \left(\frac{\alpha_0 + \left(\alpha_n + R\alpha_p\right) W_n}{W_n}\right) \qquad \tau_{PLH} = \Gamma_p \left(\frac{\alpha_0 + \left(\frac{\alpha_n}{R} + \alpha_p\right) W_p}{W_p}\right)$$

where

$$\Gamma_n = \left(\frac{L_n}{\mu_n C_{ox}}\right) \cdot \frac{2}{E_{C,n} L_n} \cdot \frac{V_{50\%}\left[\left(V_{DD} - V_{T,n}\right) + E_{C,n} L_n\right]}{\left(V_{DD} - V_{T,n}\right)^2} \qquad \Gamma_p = \left(\frac{L_p}{\mu_p C_{ox}}\right) \cdot \frac{2}{E_{C,p} L_p} \cdot \frac{V_{50\%}\left(V_{DD} - \left|V_{T,p}\right| + E_{C,p} L_p\right)}{\left(V_{DD} - \left|V_{T,p}\right|\right)^2}$$

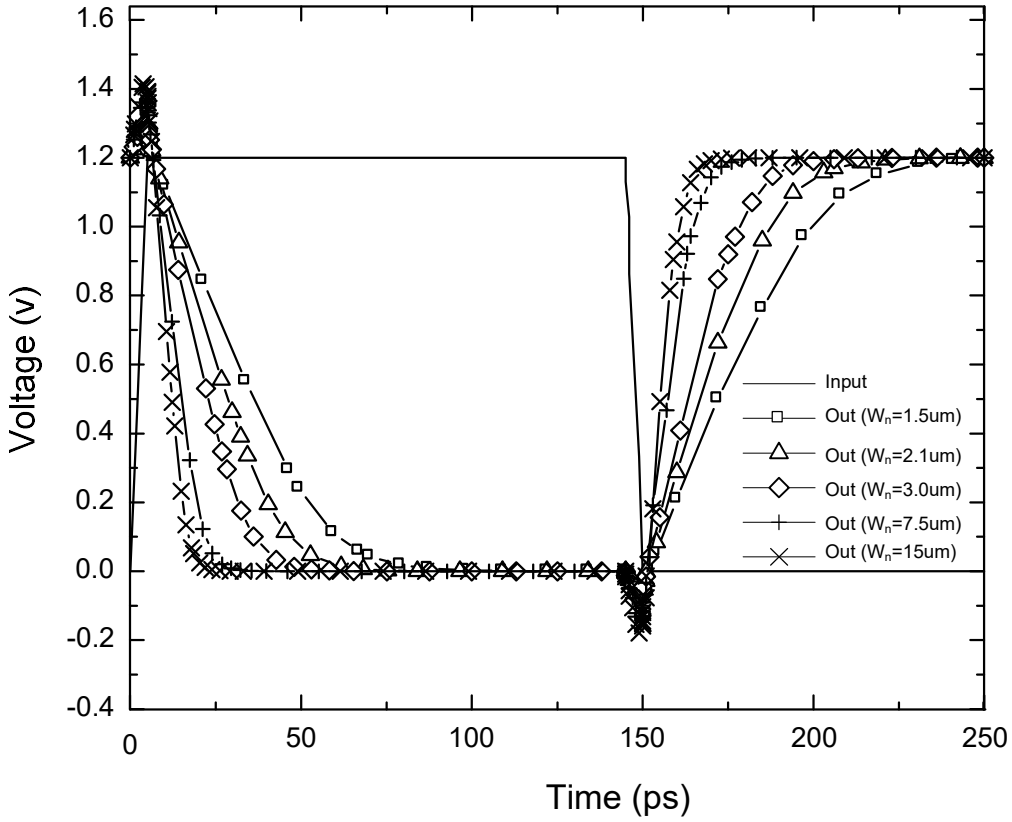
- The limit-delay values (diminishing gain)

$$\tau_{PHL}^{limit} = \Gamma_n \left(\alpha_n + R\alpha_p\right) \qquad \tau_{PLH}^{limit} = \Gamma_p \left(\frac{\alpha_n}{R} + \alpha_p\right)$$

Example 6.4 (1)

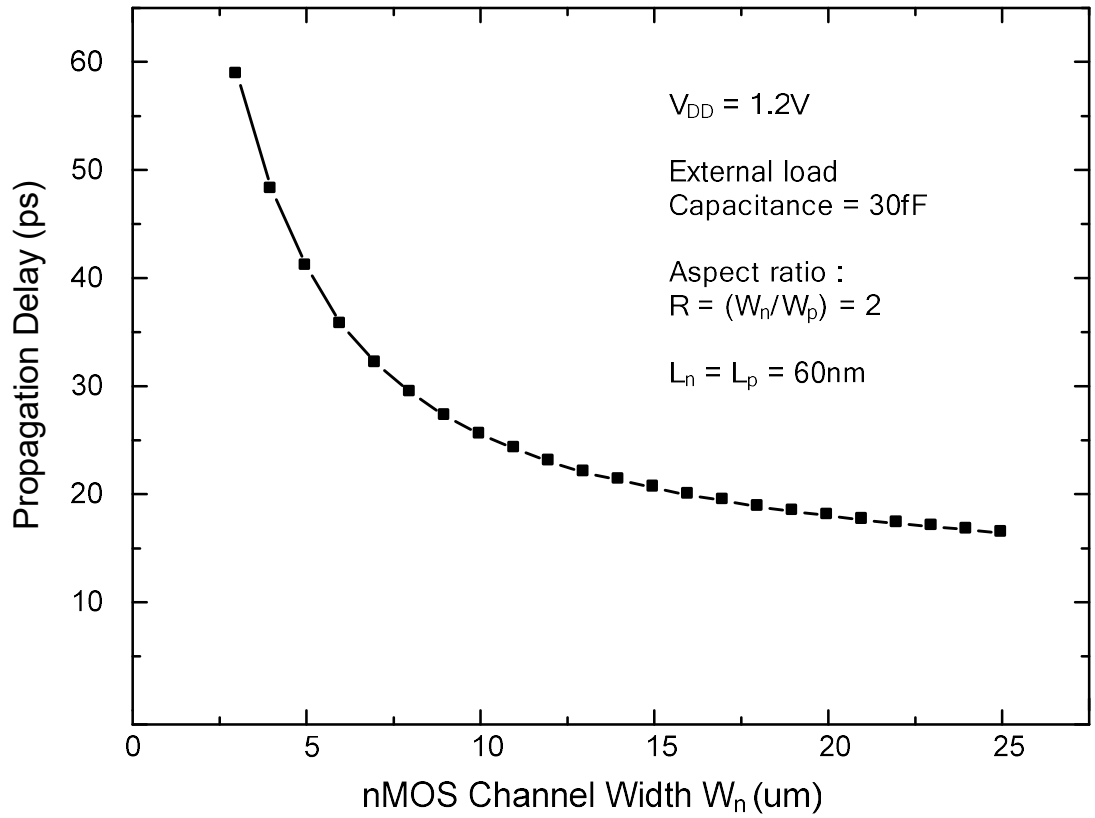
- V_{DD}=1.2V, R=(W_p/W_n)=2

◆ The simulated output voltage waveforms



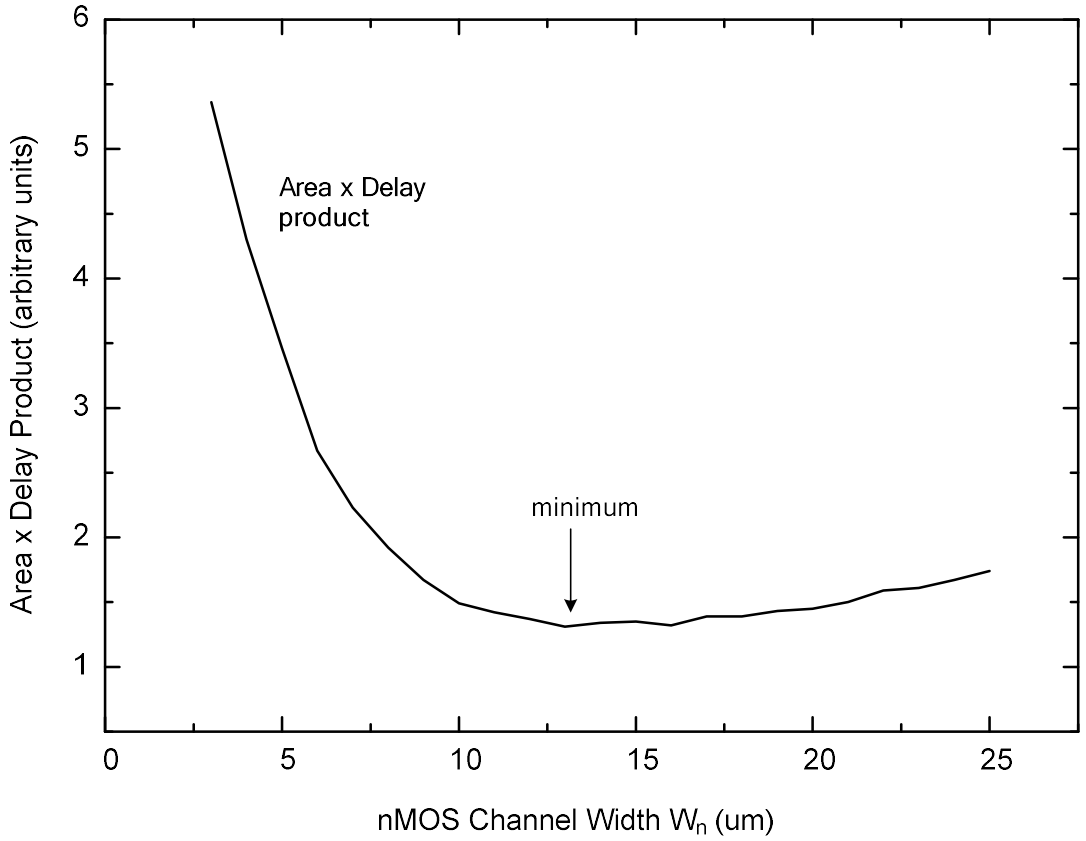
Example 6.4 (2)

- The falling-output propagation delay

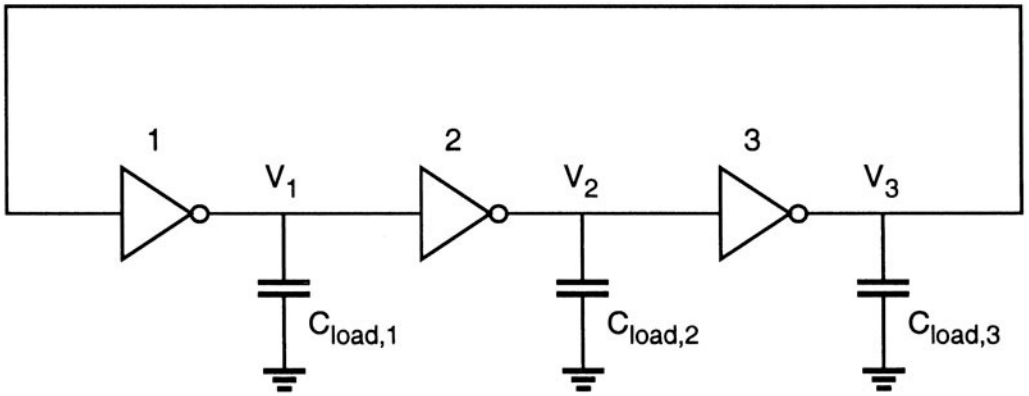


Example 6.4 (3)

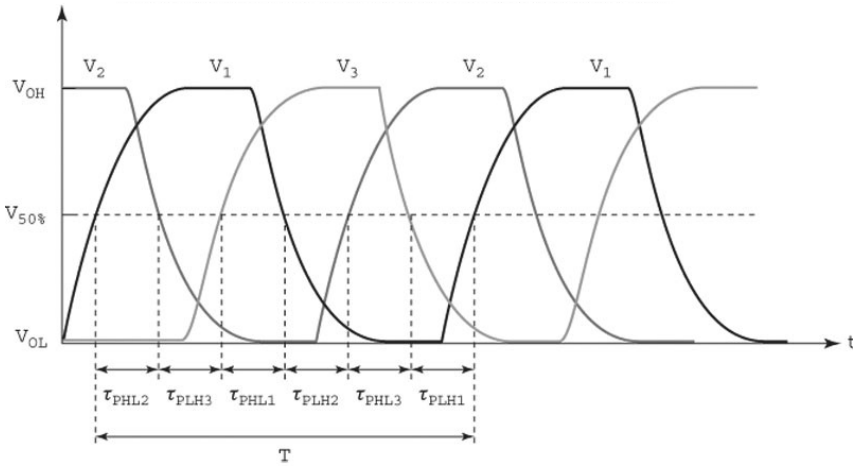
- The (Area x Delay) product



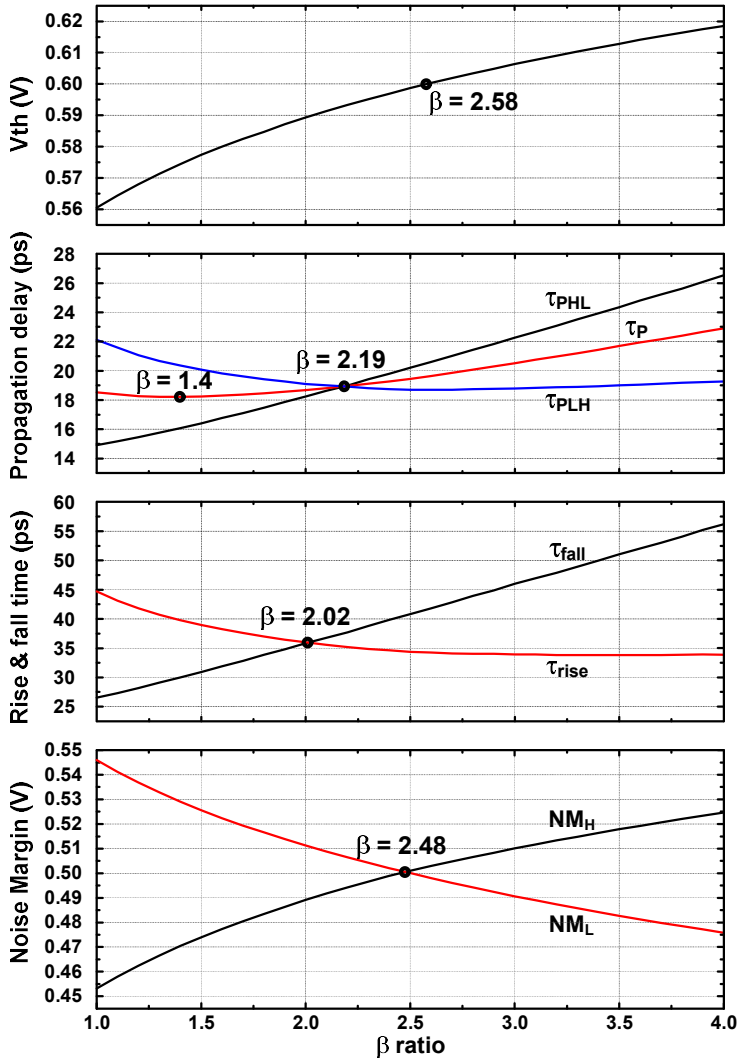
CMOS Ring Oscillator Circuit



$$T = \tau_{PHL1} + \tau_{PLH1} + \tau_{PHL2} + \tau_{PLH2} + \tau_{PHL3} + \tau_{PLH3}$$
$$= 2\tau_P + 2\tau_P + 2\tau_P$$
$$= 3 \times 2\tau_P = 6\tau_P$$

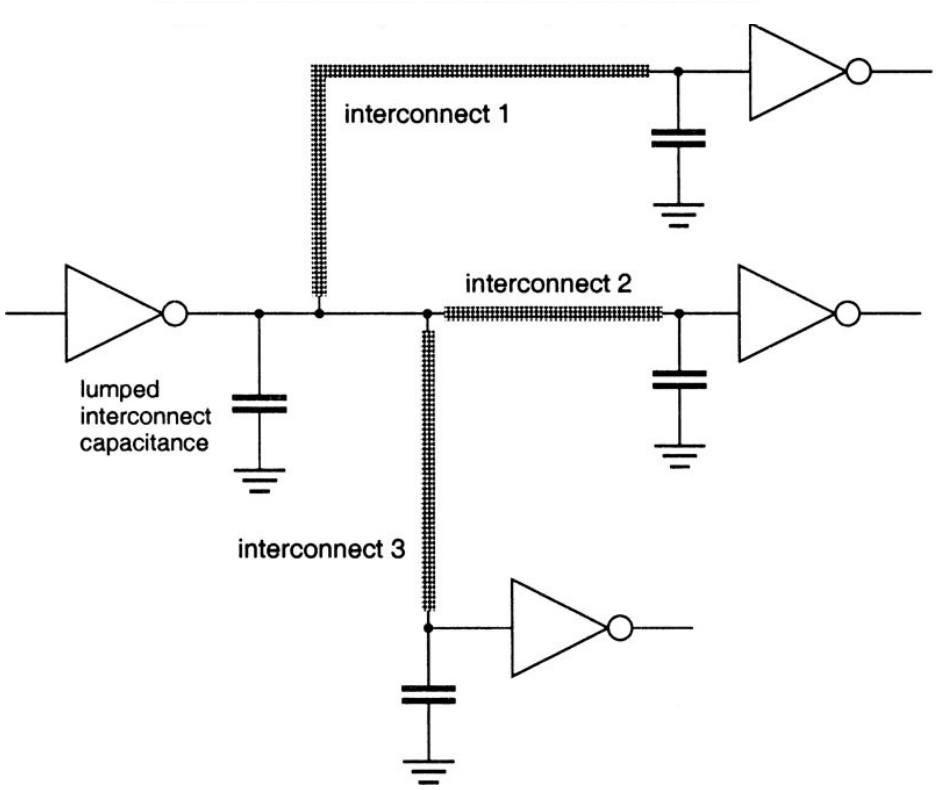


Sizing Trends of CMOS Inverter w/ Small Geometry Devices

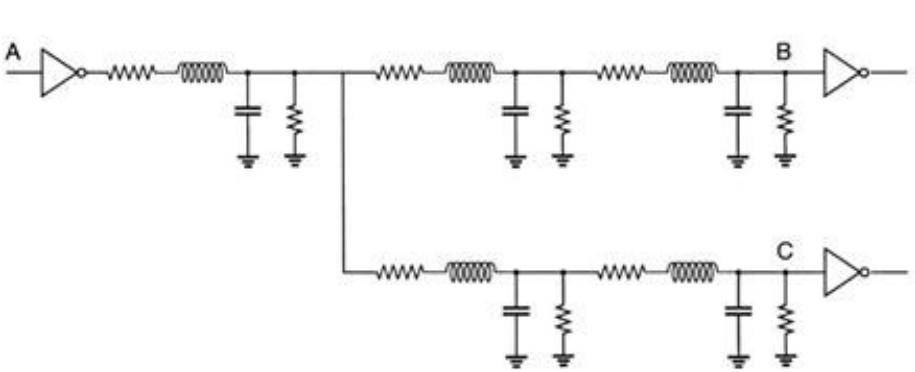


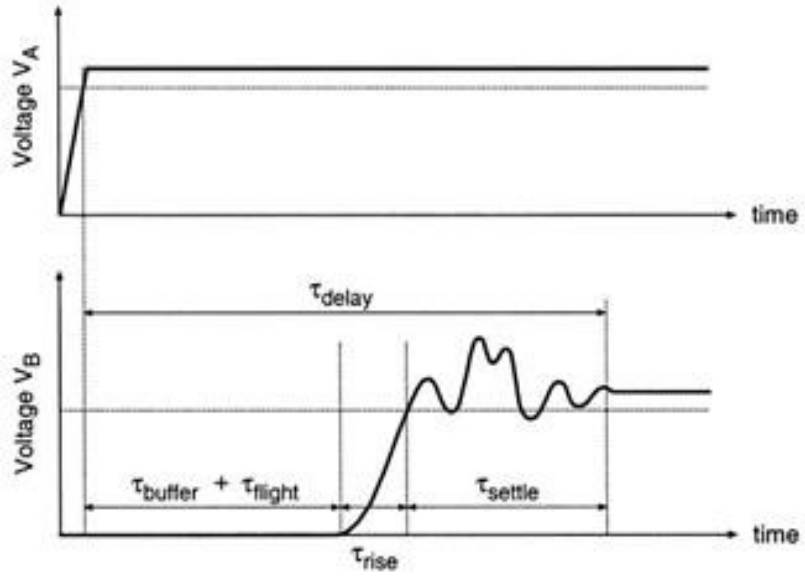
Estimation of Interconnect Parasitics

- Main components of the output load
  - Internal parasitic capacitances of transistors
  - Interconnect capacitances
  - Input capacitances of the fan-out gates



The Transmission-line Models



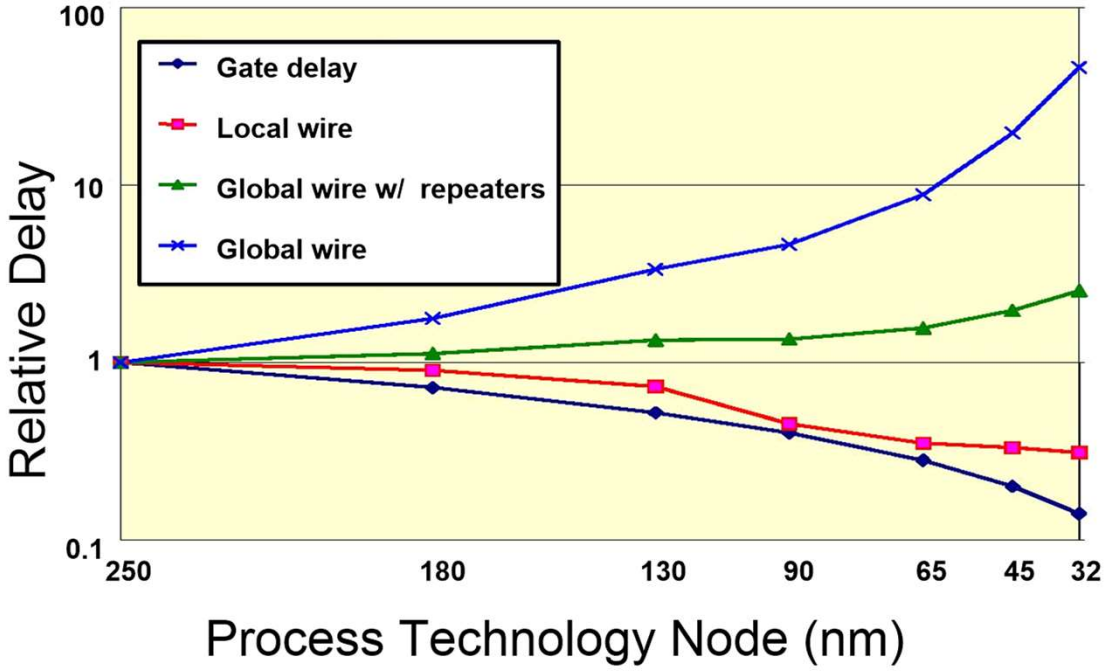


$$\tau_{rise}\left(\tau_{fall}\right) < 2.5\times\left(\frac{l}{v}\right) \quad \Rightarrow \{\text{transmission-line modeling}\}$$

$$2.5\times\left(\frac{l}{v}\right) < \tau_{rise}\left(\tau_{fall}\right) < 5\times\left(\frac{l}{v}\right) \Rightarrow \left\{\begin{matrix}\text{either transmission-line} \\ \text{or lumped modeling}\end{matrix}\right\}$$

$$\tau_{rise}\left(\tau_{fall}\right) > 5\times\left(\frac{l}{v}\right) \quad \Rightarrow \{\text{lumped modeling}\}$$

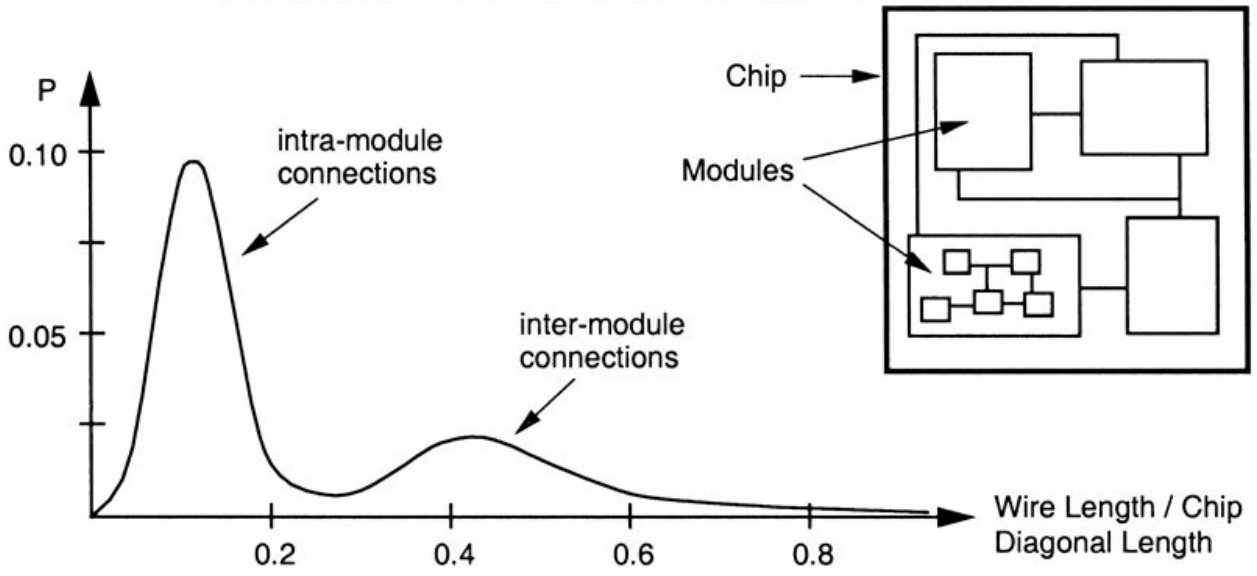
Interconnect Delay



- Dealing with the implications and optimizing a system for speed
  - Estimating the interconnect parasitics in a large chip
  - Simulating the transient effects.

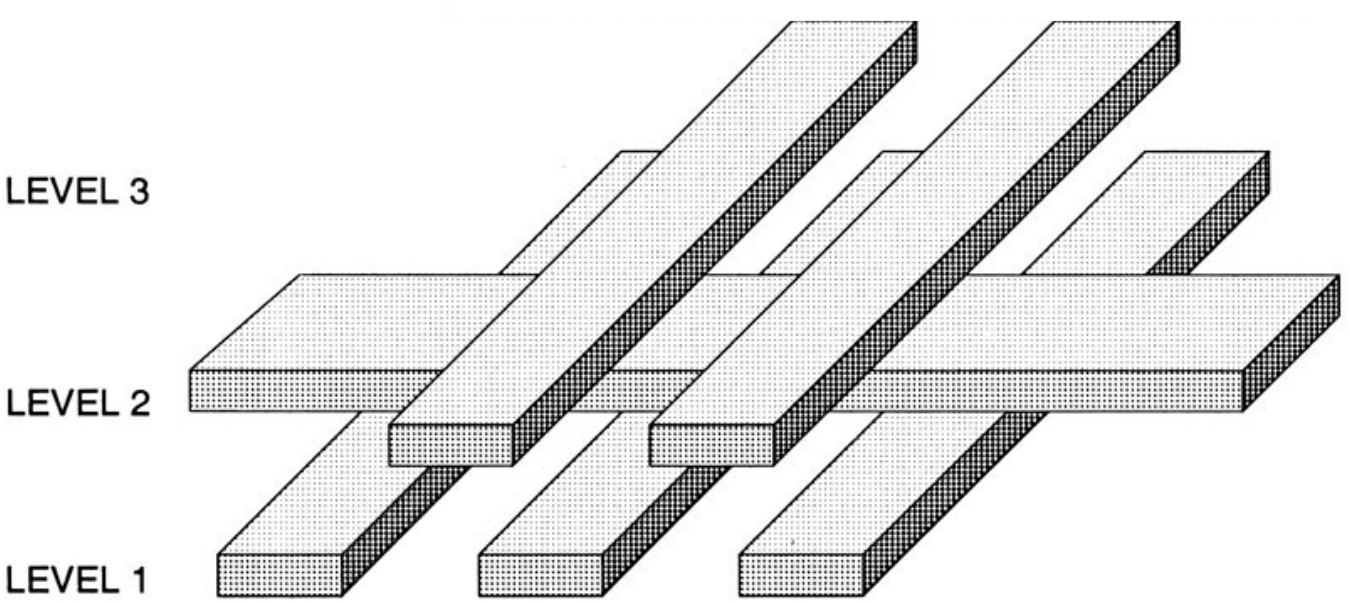
Statistical distribution

- Statistical distribution of interconnection length on a typical chip



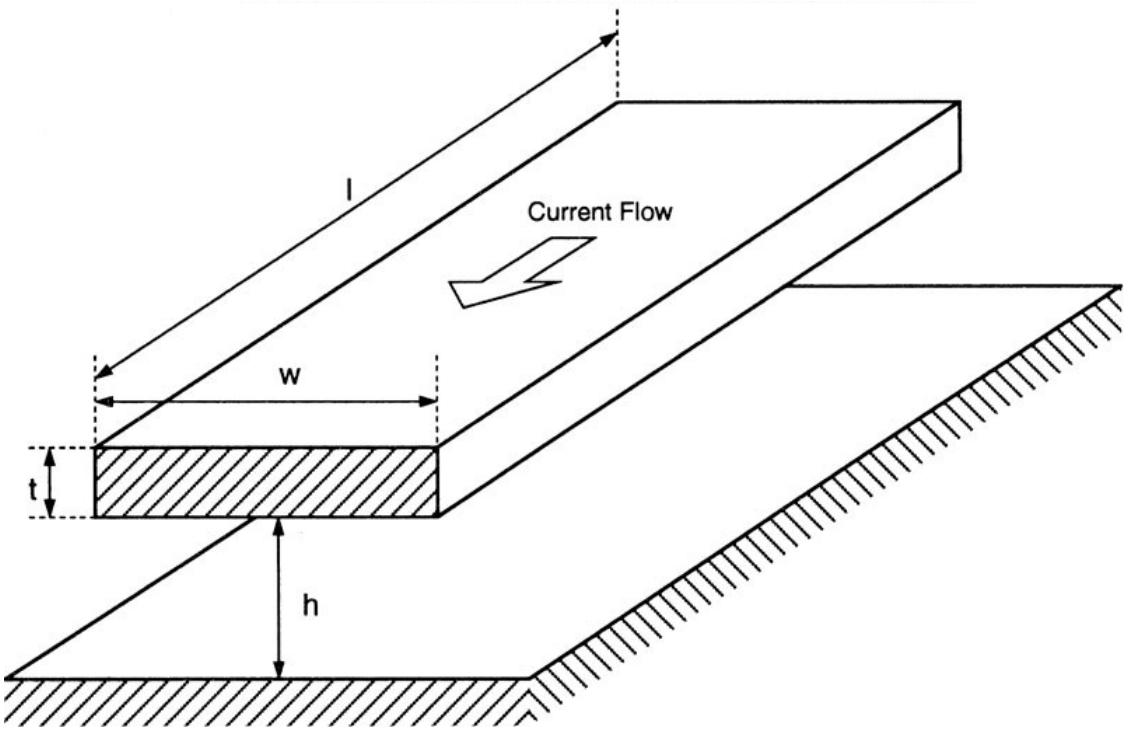
Interconnect Capacitance Estimation (1)

- A simplified view of six interconnections on three different levels



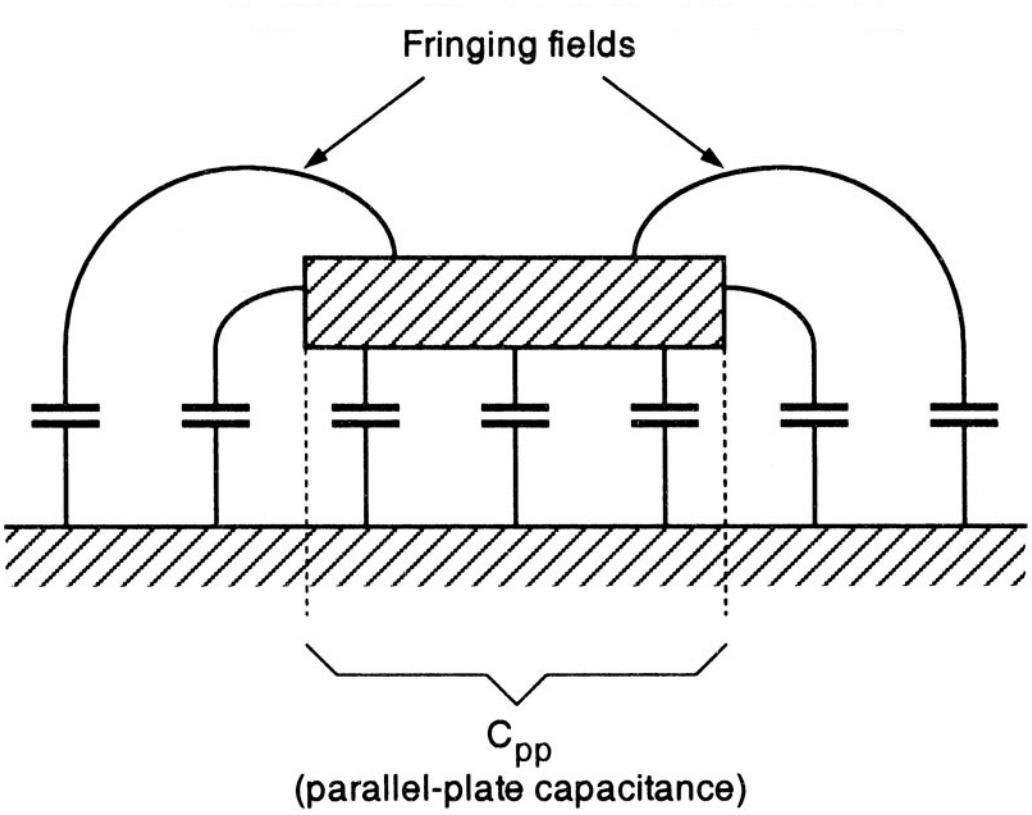
Interconnect Capacitance Estimation (2)

- The section of a single interconnect



Interconnect Capacitance Estimation (3)

- The total parasitic capacitance



Thickness value of different layers

Field oxide thickness	**3µm**	
Gate oxide thickness	**2.6nm**	
Polysilicon thickness	**1µm**	**(minimum width 0.06µm)**
Poly-metal oxide thickness	**1.1µm**	
Metal 1 thickness	**1.8µm**	**(minimum width 0.09µm)**
Metal 2~7 thickness	**2.2µm**	**(minimum width 0.1µm)**
Metal 8~9 thickness	**9µm**	**(minimum width 0.4µm)**
Via oxide thickness (PO-M1)	**1.75µm**	
Via oxide thickness (M1-M6)	**2.2µm**	
Via oxide thickness (M6-M9)	**9µm**	
n^+ junction depth	**23nm**	
p^+ junction depth	**28nm**	
n-well junction depth	**3µm**	

Parasitic Parallel-plate capacitance values

	FOX	PO	M1	M2	M3	M4	M5	M6	M7	M8	M9
FOX	-	6.37	5.14	2.98	1.99	1.49	1.20	0.99	0.85	3.23	2.45
PO	6.37	-	16.6	5.13	1.99	1.49	1.44	1.16	0.97	3.57	2.64
M1	5.14	16.6	-	15.1	4.28	2.50	1.76	1.36	1.11	3.96	2.85
M2	2.98	5.13	15.1	-	15.1	4.28	2.50	1.76	1.36	4.61	3.17
M3	1.99	1.99	4.28	15.1	-	15.1	4.28	2.50	1.76	5.51	3.57
M4	1.49	1.49	2.50	4.28	15.1	-	15.1	4.28	2.50	6.85	4.09
M5	1.20	1.44	1.76	2.50	4.28	15.1	-	15.1	4.28	9.05	4.79
M6	0.99	1.16	1.36	1.76	2.50	4.28	15.1	-	15.1	13.3	5.77
M7	0.85	0.97	1.11	1.36	1.76	2.50	4.28	15.1	-	25.3	7.26
M8	3.23	3.57	3.96	4.61	5.51	6.85	9.05	13.3	25.3	-	25.3
M9	2.45	2.64	2.85	3.17	3.57	4.09	4.79	5.77	7.26	25.3	-

Parasitic Fringing-plate capacitance values

	FOX	PO	M1	M2	M3	M4	M5	M6	M7	M8	M9
FOX	-	23.4	15.1	13.2	11.5	10.7	10.2	10.4	10.5	12.3	11.2
PO	23.4	-	27.6	15.6	12.6	11.4	10.4	10.4	10.9	12.7	11.2
M1	15.1	27.6	-	26.4	14.5	12.3	11.3	10.8	11.3	13.2	11.8
M2	13.2	15.6	26.4	-	26.4	14.6	12.4	11.6	11.9	13.9	12.3
M3	11.5	12.6	14.5	26.4	-	26.4	14.7	12.7	12.7	14.9	12.8
M4	10.7	11.4	12.3	14.6	26.4	-	26.4	14.9	13.9	16.4	13.5
M5	10.2	10.4	11.3	12.4	14.7	26.4	-	26.8	16.4	18.6	14.3
M6	10.4	10.4	10.8	11.6	12.7	14.9	26.8	-	28.6	22.6	15.3
M7	10.5	10.9	11.3	11.9	12.7	13.9	16.4	28.6	-	33.0	16.7
M8	12.3	12.7	13.2	13.9	14.9	16.4	18.6	22.6	33.0	-	32.4
M9	11.2	11.2	11.8	12.3	12.8	13.5	14.3	15.3	16.7	32.4	-

Interconnect Resistance Estimation

- Total resistance in indicated current direction

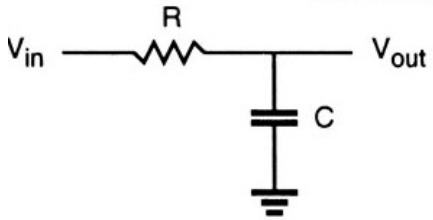
$$R_{wire} = \rho \cdot \frac{l}{w \cdot t} = R_{sheet}\left(\frac{l}{w}\right)$$

- The sheet resistivity of the line

$$R_{sheet} = \left(\frac{\rho}{t}\right)$$

RC Delay Models

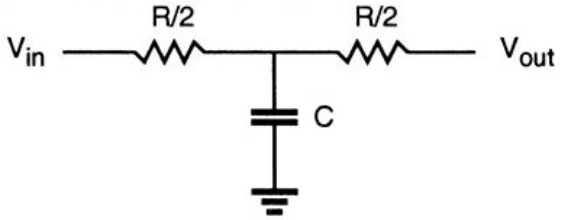
- Simple lumped RC model & T-model



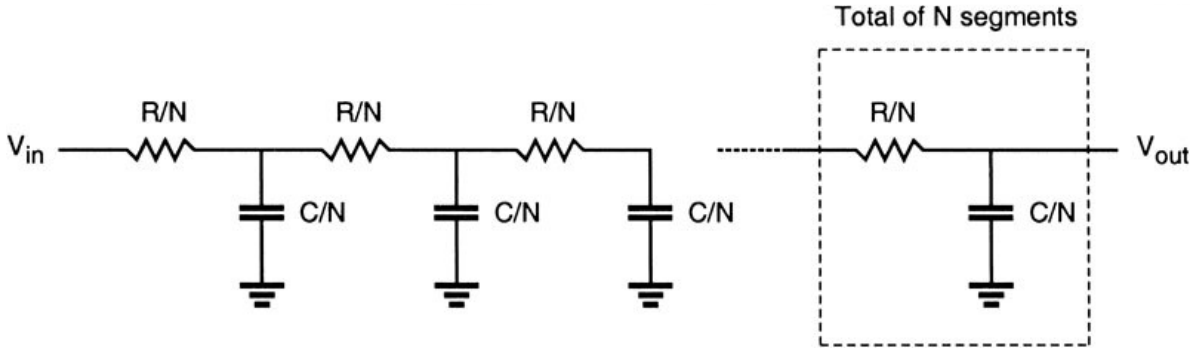
$$V_{out}(t) = V_{DD}\left(1 - exp\left(-\frac{t}{RC}\right)\right)$$

$$V_{50\%} = V_{DD}\left(1 - exp\left(-\frac{\tau_{PLH}}{RC}\right)\right)$$

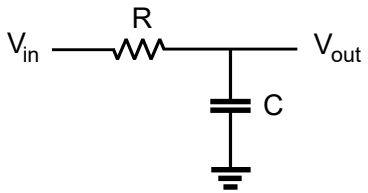
$$\tau_{PLH} \approx 0.69RC$$



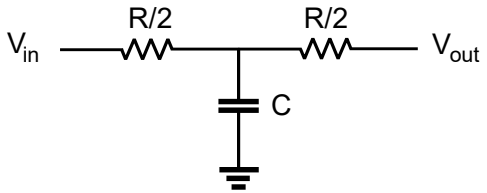
- Distributed RC ladder network model



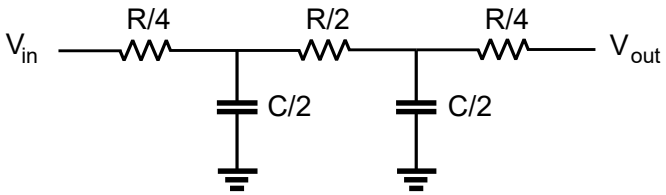
Various RC Models



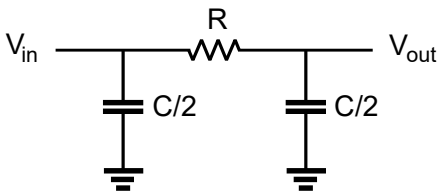
(a) lumped RC model



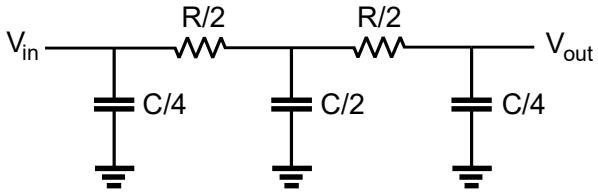
(b) T-model



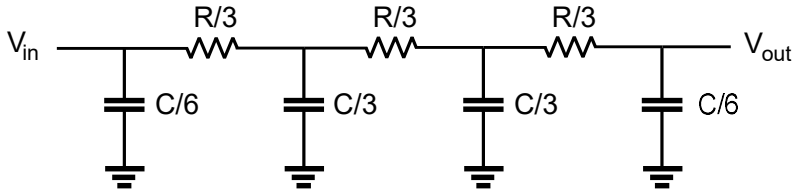
(c) T2-model



(d) π-model

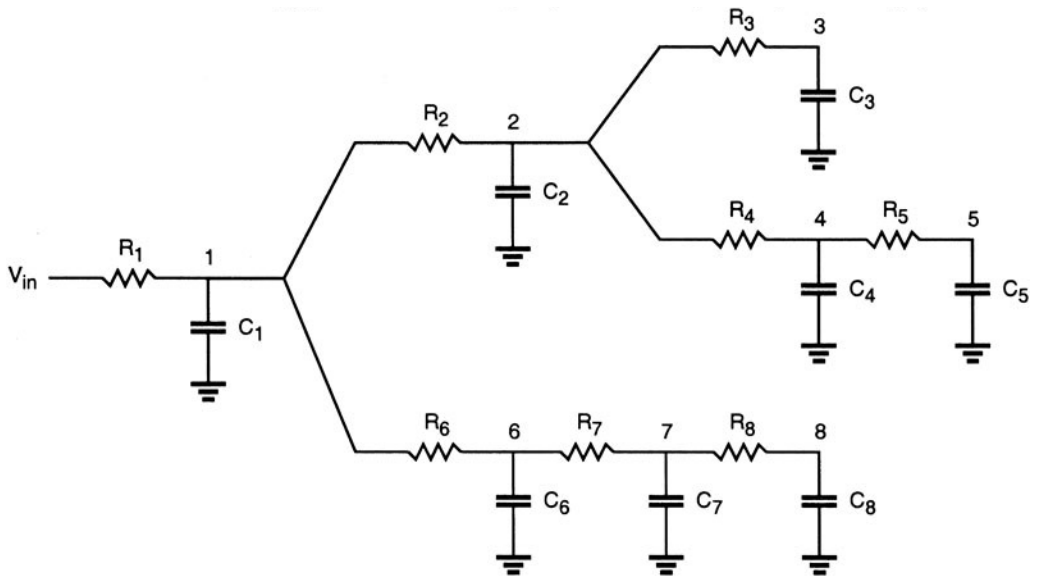


(e) π2-model



(f) π3-model

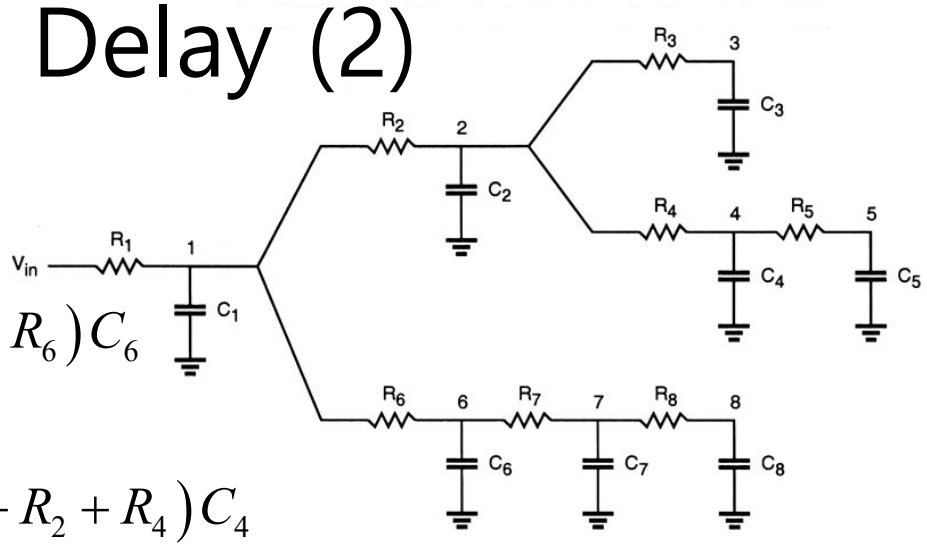
The Elmore Delay (1)



$$\tau_{Di} = \sum_{j=1}^{N} C_j \sum_{\substack{for\ all \\ k \in P_{ij}}} R_k$$

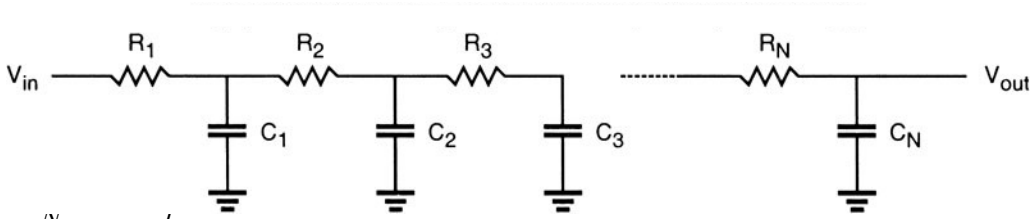
- The general topology of the RC tree network
  - Let *Pi* denote the unique path from the input node to node *i*, *i* = 1, 2, 3, ..., N.
  - Let *Pij* = *Pi* « *Pj* denote the portion of the path between the input and the node *i*, which is *common* to the path between the input and node *j*.

The Elmore Delay (2)



$$\tau_{D7} = R_1C_1 + R_1C_2 + R_1C_3 + R_1C_4 + R_1C_5 + (R_1 + R_6)C_6 + (R_1 + R_6 + R_7)C_7 + (R_1 + R_6 + R_7)C_8$$

$$\tau_{D5} = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2)C_3 + (R_1 + R_2 + R_4)C_4 + (R_1 + R_2 + R_4 + R_5)C_5 + R_1C_6 + R_1C_7 + R_1C_8$$



$$\tau_{DN} = \sum_{j=1}^{N} C_j \sum_{k=1}^{J} R_k \qquad \tau_{DN} = \sum_{j=1}^{N}\left(\frac{C}{N}\right)\sum_{k=1}^{j}\left(\frac{R}{N}\right)$$

$$= \left(\frac{C}{N}\right)\left(\frac{R}{N}\right)\left(\frac{N(N+1)}{2}\right) = RC\left(\frac{N+1}{2N}\right)$$

$$\tau_{DN} = \frac{RC}{2} \quad for \quad N \to \infty$$

Example 6.5 (1)

- 1) Examine the propagation delay across a long polysilicon interconnect line (length=1000 μ m, width=1 μ m)
  - R_{sheet}= 15 Ω/square
- 1) Sol.

$$R_{lumped} = R_{sheet} \times (\#\ \text{of squares})$$

$$= 15(\Omega/\text{square}) \times \left(\frac{1000\mu\text{m}}{1\mu\text{m}} \right) = 15\text{k}\Omega$$

$$C_{parallel-plate} = (\text{unit area capacitance}) \times (\text{area})$$

$$= 0.106\text{fF}/\mu\text{m}^2 \times (1000\mu\text{m} \times 1\mu\text{m}) = 106\text{fF}$$

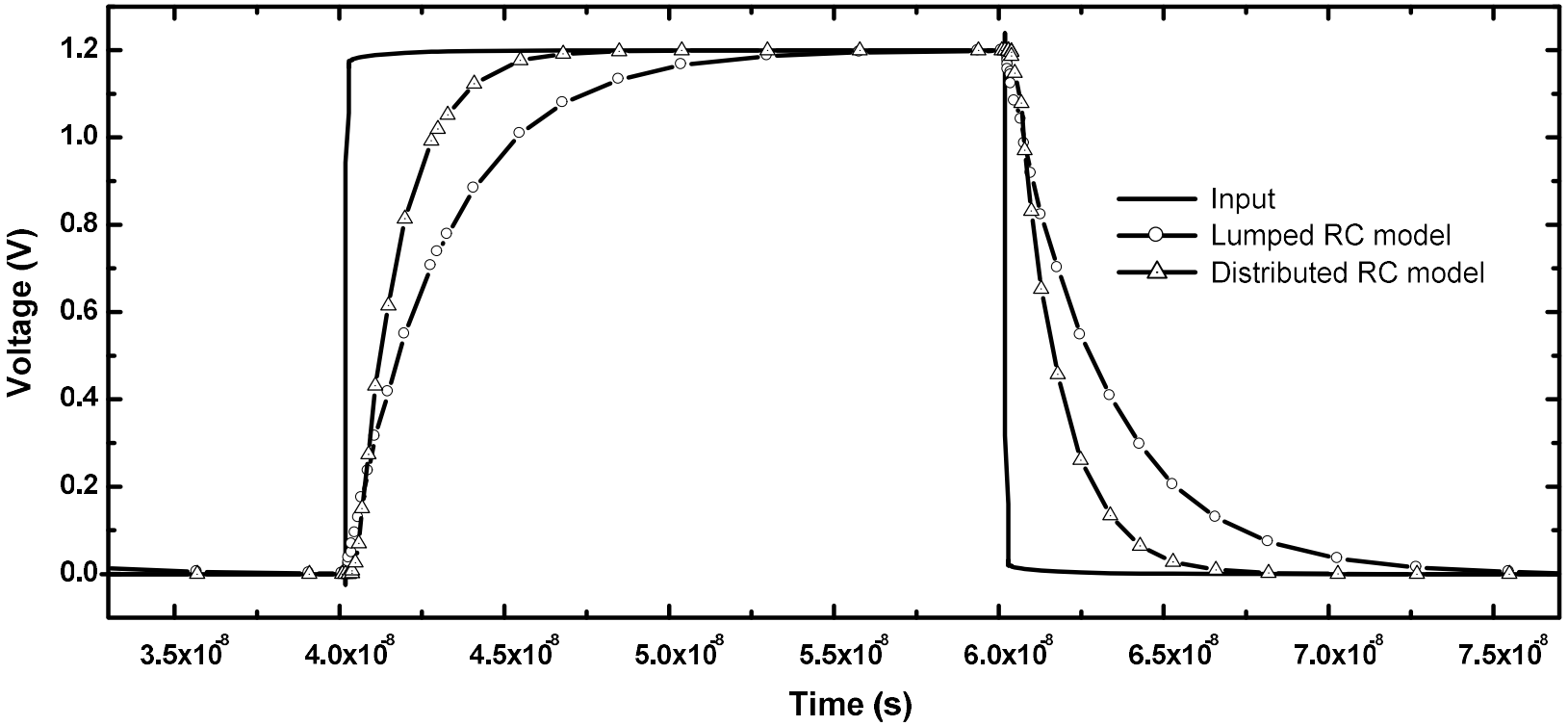
$$C_{fringe} = (\text{unit length capacitance}) \times (\text{perimeter})$$

$$= 0.043\text{fF}/\mu\text{m} \times (1000\mu\text{m} + 1000\mu\text{m} + 1\mu\text{m} + 1\mu\text{m}) = 86\text{fF}$$

$$C_{lumped-total} = C_{parallel-plate} + C_{fringe} = 192\text{fF}$$

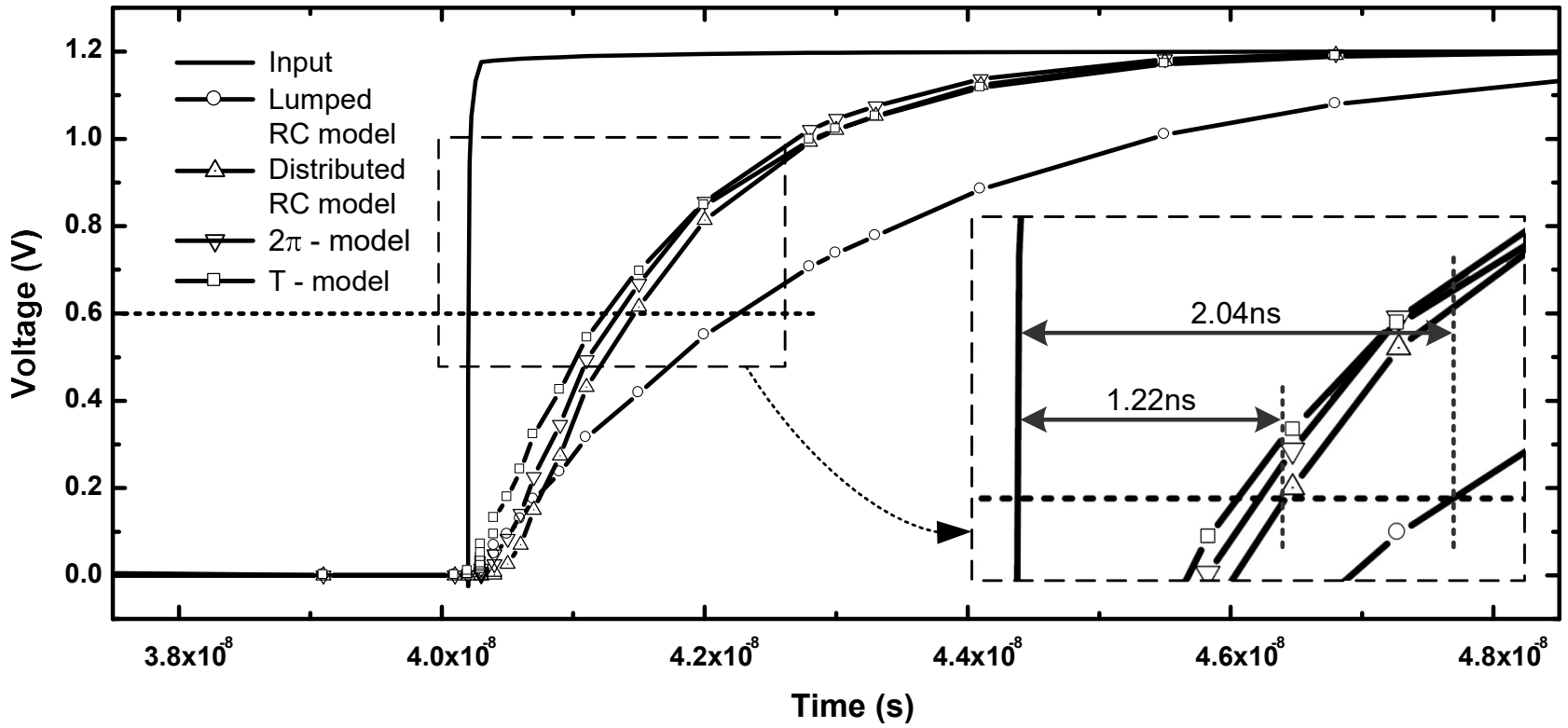
Example 6.5 (2)

- The simulated output voltage waveforms



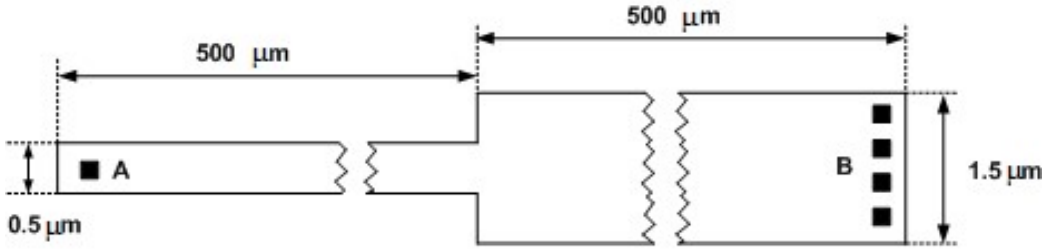
Example 6.5 (3)

- The simulated output voltage waveforms with an overestimation of the propagation delay time



Example 6.5 (4)

- 2) Consider a polysilicon line consisting of two segments (W=1.5 μm & W=0.5 μm, each 500 μm)



polysilicon interconnect line

- 2) Sol.

$$R_{lumped-1} = 15(\Omega/\text{square}) \times \left(\frac{500\mu\text{m}}{0.5\mu\text{m}}\right) = 15\text{k}\Omega,\ R_{lumped-2} = 15(\Omega/\text{square}) \times \left(\frac{500\mu\text{m}}{1.5\mu\text{m}}\right) = 5\text{k}\Omega$$

$$R_{lumped-total} = R_{lumped-1} + R_{lumped-2} = 20\text{k}\Omega$$

$$C_{parallel-plate-1} = 0.106\text{fF}/\mu\text{m}^2 \times (500\mu\text{m} \times 0.5\mu\text{m}) = 26.5\text{fF}$$

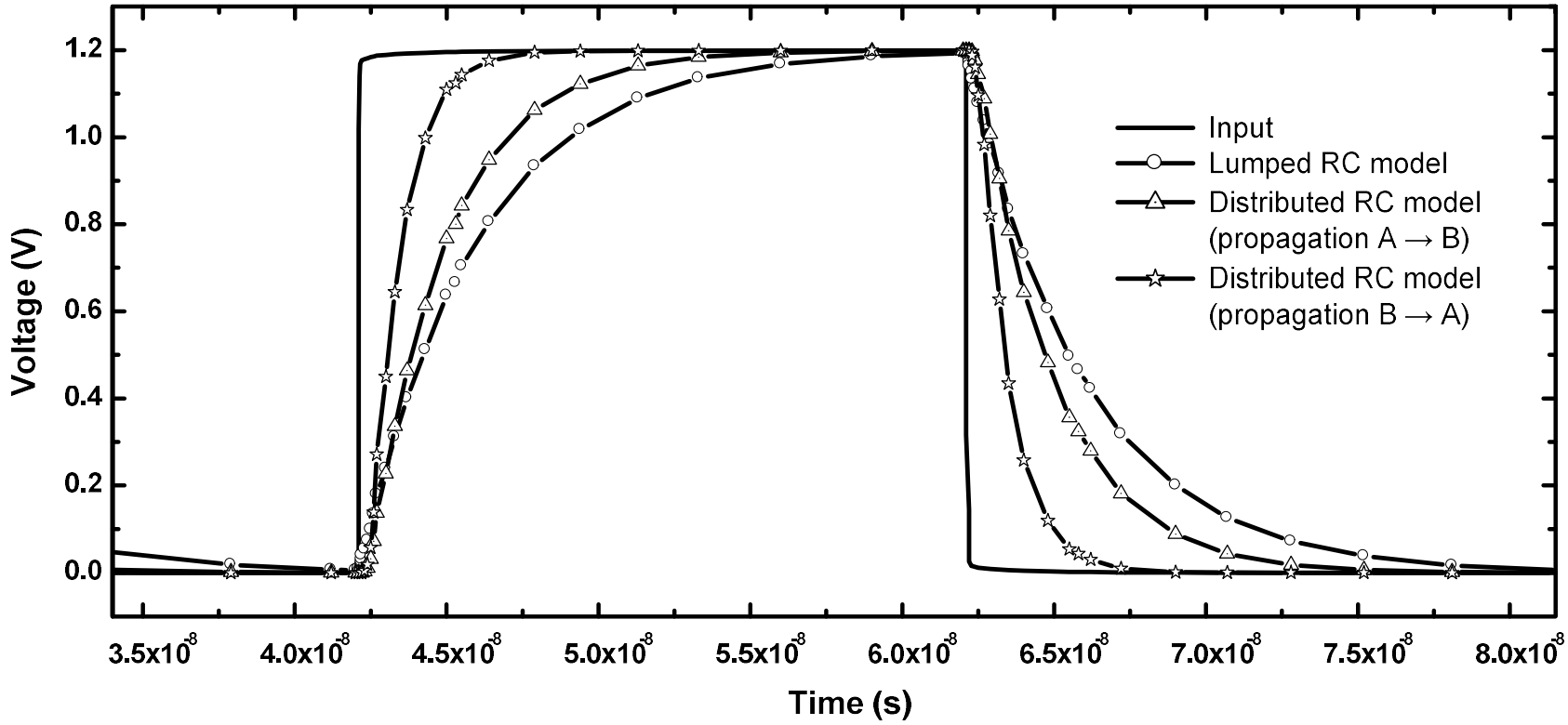
$$C_{parallel-plate-2} = 0.106\text{fF}/\mu\text{m}^2 \times (500\mu\text{m} \times 1.5\mu\text{m}) = 79.5\text{fF}$$

$$C_{fringe-1} \approx C_{fringe-2} = 46\text{fF}$$

$$C_{lumped-total} = C_{parallel-plate-1} + C_{parallel-plate-2} + C_{fringe-1} + C_{fringe-2} = 192\text{fF}$$

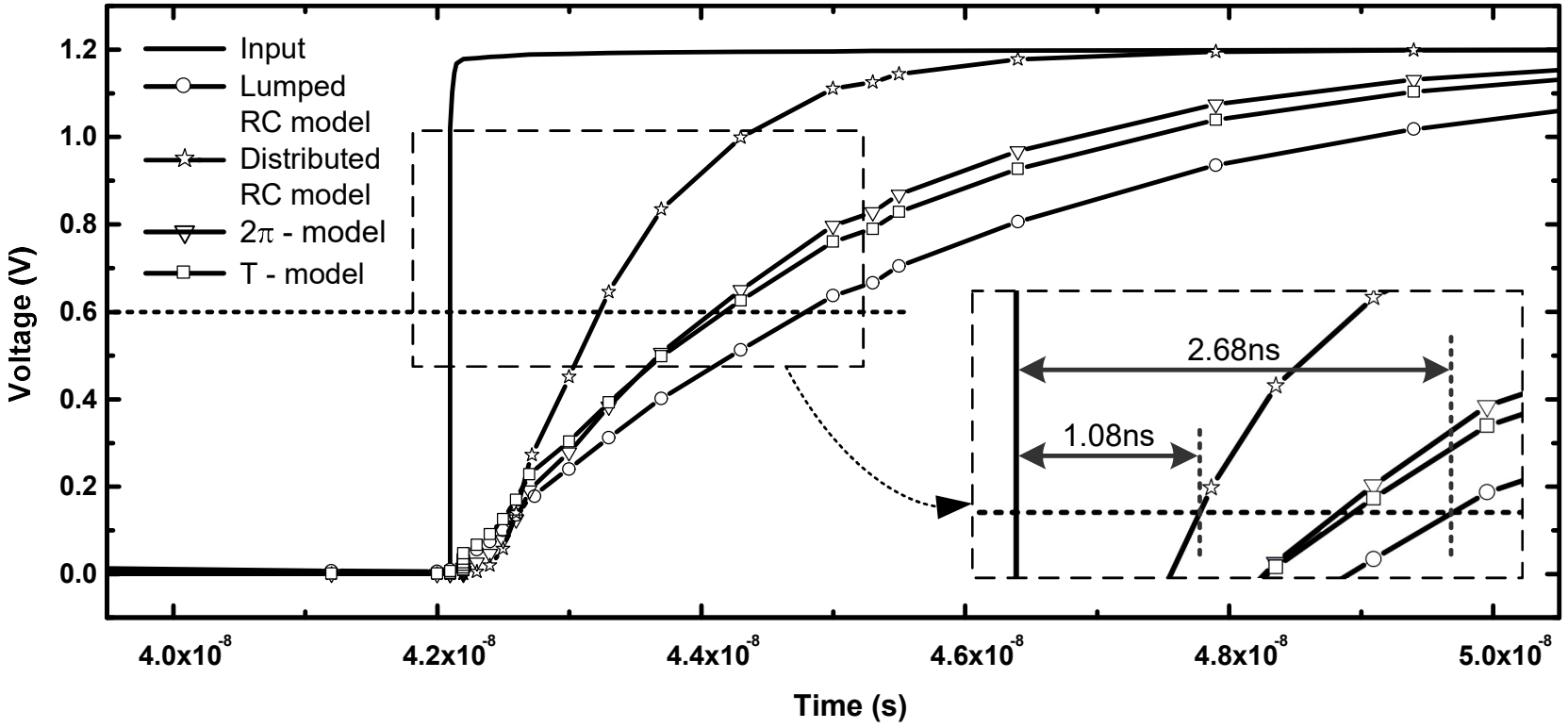
Example 6.5 (5)

- The simulated output voltage waveforms

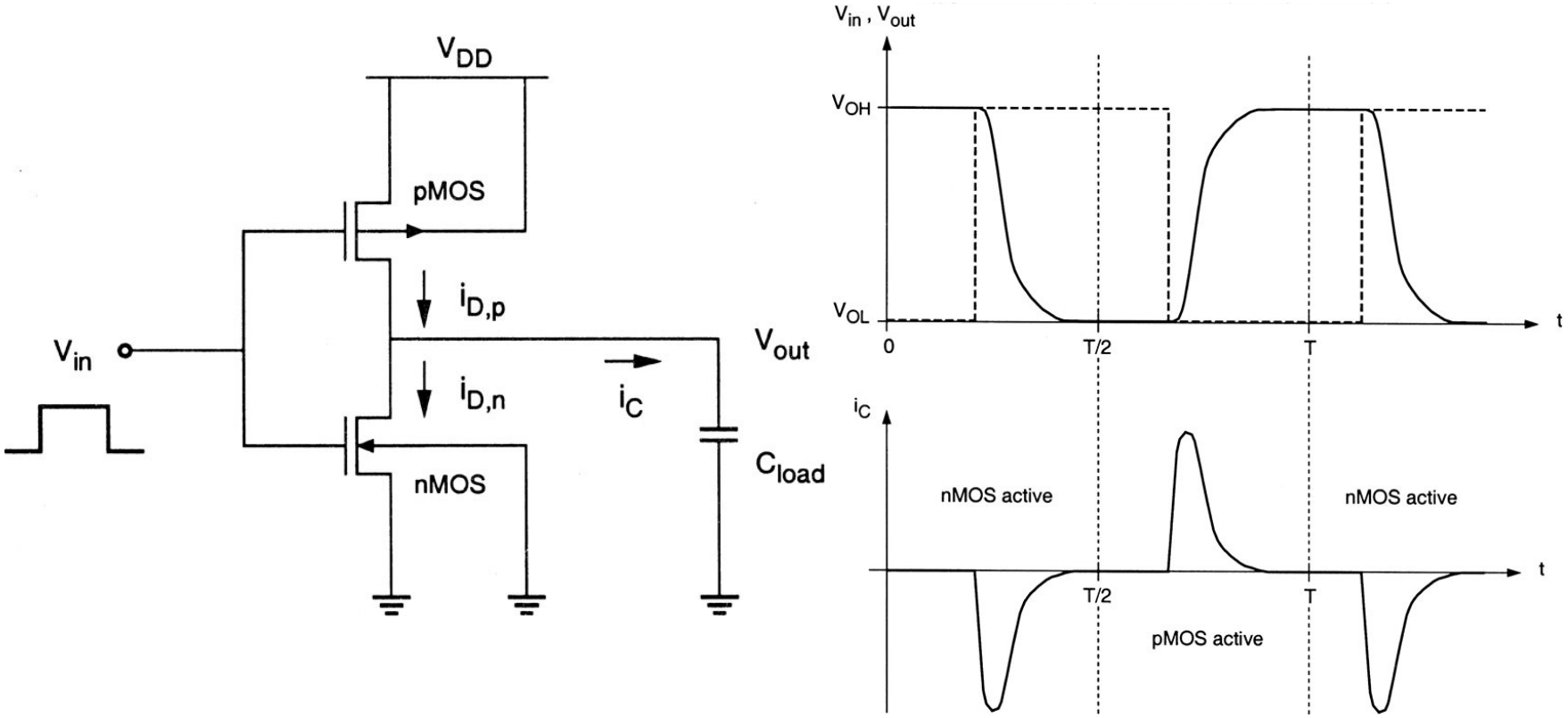


Example 6.5 (6)

- The simulated output voltage waveforms with an overestimation of the propagation delay time



Switching Power Dissipation



The Average Power Dissipation

$$P_{avg} = \frac{1}{T}\int_0^T v(t)\cdot i(t)\,dt$$

- The average power dissipation of CMOS inverters

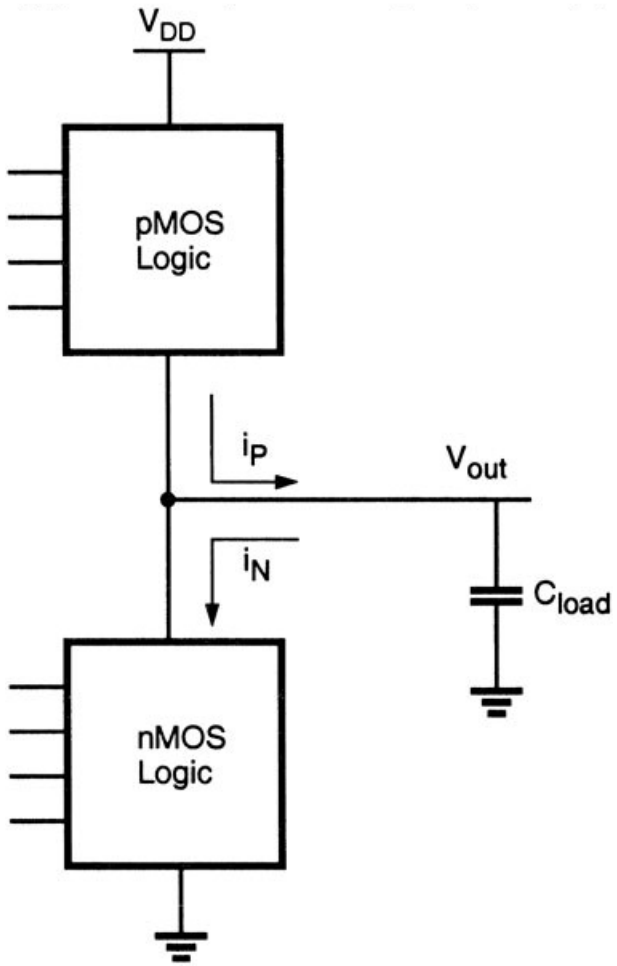
$$P_{avg} = \frac{1}{T}\left[\int_0^{T/2} V_{out}\left(-C_{load}\frac{dV_{out}}{dt}\right)dt + \int_{T/2}^{T}(V_{DD}-V_{out})\left(C_{load}\frac{dV_{out}}{dt}\right)dt\right]$$

$$P_{avg} = \frac{1}{T}\left[\left(-C_{load}\frac{V_{out}^2}{2}\right)\Bigg|_0^{T/2} + \left(V_{DD}\cdot V_{out}\cdot C_{load} - \frac{1}{2}C_{load}V_{out}^2\right)\Bigg|_{T/2}^{T}\right]$$

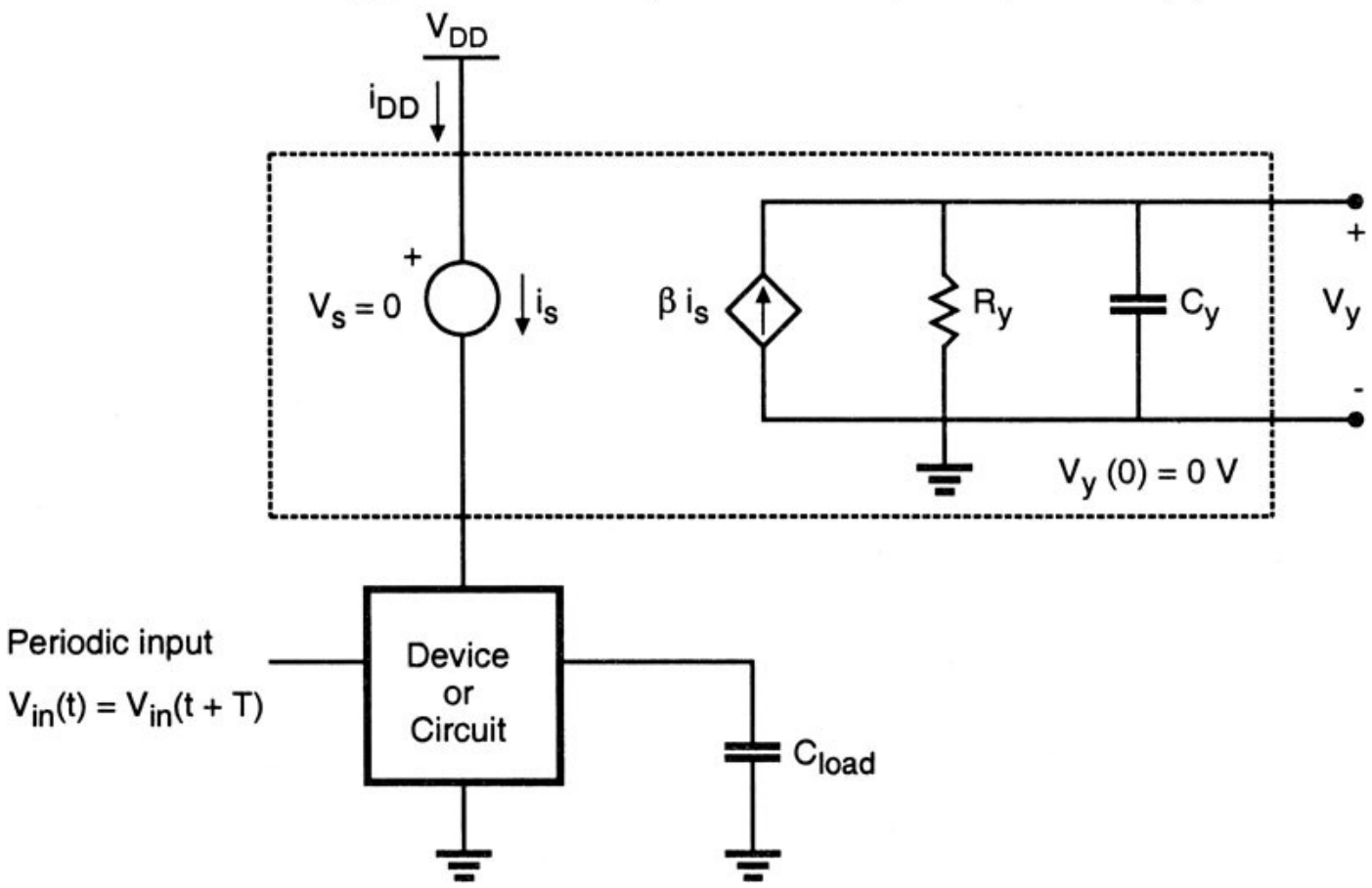
$$P_{avg} = \frac{1}{T}C_{load}V_{DD}^2 \quad \text{or} \quad P_{avg} = C_{load}\cdot V_{DD}^2\cdot f$$

The Switching Power Expression

- The average switching power expression will hold for any CMOS logic circuit.



Power Meter Simulation (1)



Power Meter Simulation (2)

- The current equation for the common node

$$C_y \frac{dV_y}{dt} = \beta i_s - \frac{V_y}{R_y}$$

- The initial condition of V_y

$$V_y(t) = \frac{\beta}{C_y} \int_0^t exp\left(-\frac{t-\tau}{R_y C_y}\right) i_{DD}(\tau)\, d\tau$$

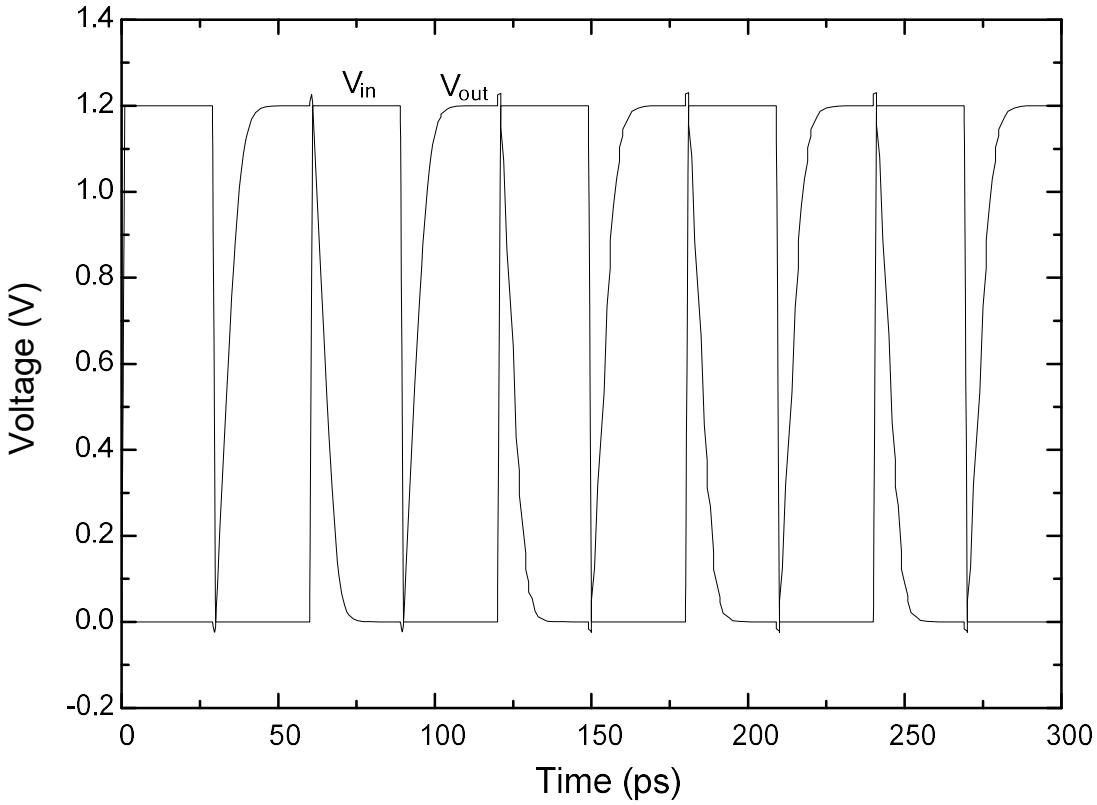
- Assuming $R_y C_y \gg T$,

$$V_y(T) \approx \frac{\beta}{C_y} \int_0^T i_{DD}(\tau) d\tau \qquad \beta = V_{DD} \frac{C_y}{T}$$

$$V_y(T) = V_{DD} \cdot \frac{1}{T} \int_0^T i_{DD}(\tau) d\tau$$

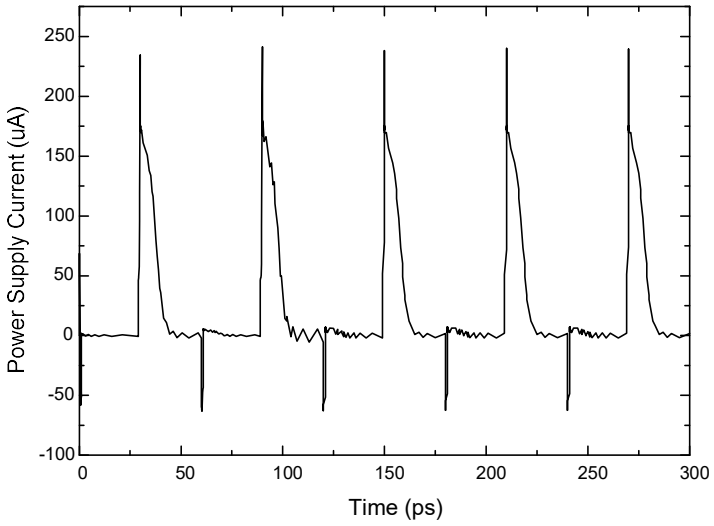
Example 6.6 (1)

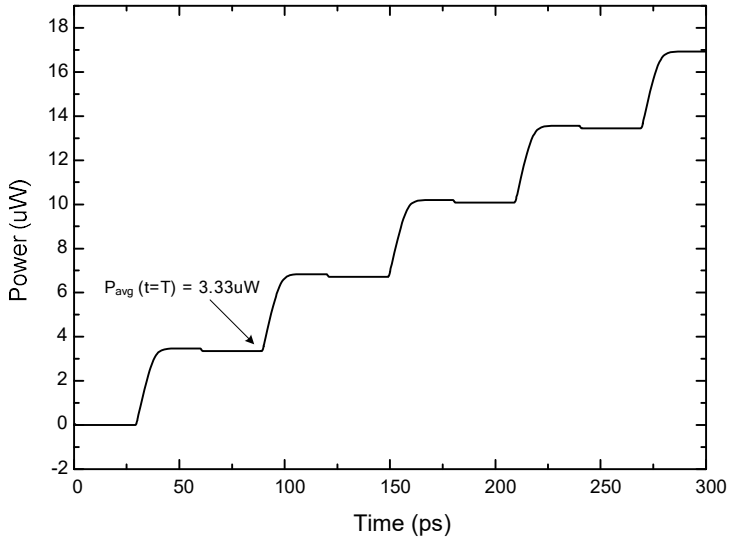
- Simulate the Circuit in Fig. 6.27 w/ power meter
  - V_{DD}=1.2V, P_{avg}=0.25mW



Example 6.6 (2)

- Simulation results





Power-Delay Product

- The average dynamic power dissipation

$$PDP = C_{load} V_{DD}^2$$

- The power-delay product

$$PDP = 2 P_{avg}^* \tau_P$$

$$PDP = 2\left(C_{load} V_{DD}^2 f_{max} \right) \tau_P$$

$$= 2\left[C_{load} V_{DD}^2 \left(\frac{1}{\tau_{PHL} + \tau_{PLH}} \right) \right] \left(\frac{\tau_{PHL} + \tau_{PLH}}{2} \right)$$

$$= C_{load} V_{DD}^2$$

Energy-Delay Product

- A fair metric for comparison

	Delay (ps)	Power consumption (mW)	PDP (pJ)	EDP (10^{-21}J·s)
Add_a	180	40	7.2	1.296
Add_b	240	30	7.2	1.728

- EDP

$$EDP = PDP \times \tau_p$$
$$= C_{load} V_{DD}^2 \tau_p$$
$$= 2P_{avg}^* \tau_P^2$$