Power $< \frac{1}{2} C V_{DD}^2 f_{clock}$

$V_{DD}$ is most critical.

For instance, if $V_{DD} \rightarrow \frac{1}{2} V_{DD}$

Power is reduced to $\frac{1}{4}$ (50% saving)

In pipelining, each stage can use

$V_{DD} = \frac{V_{DD}}{2}$

Thus $n \times \frac{V_{DD}}{2} \rightarrow$ power saving $\frac{1}{2^n}$

Reducing Power through Pipelining

\[ \begin{align*}
\text{Input} & \quad F(X) \quad \text{Output} \\
\text{CLK} & \quad \text{CLK} \\
\text{CLK} & \quad \text{CLK} \\
\text{CLK} & \quad \text{CLK} \\
\text{CLK} & \quad \text{CLK} \\
\text{CLK} & \quad \text{CLK} \\
\text{CLK} & \quad \text{CLK} \\
\text{CLK} & \quad \text{CLK} \\
\end{align*} \]

\[ \frac{P_{Total}}{C_{Total}} = \frac{5V}{0.8V} \cdot \frac{4V}{4V} \cdot \frac{4V}{4V} = 0.1 \]

\[ \left( 1 + \frac{N}{C_{Total}} \frac{1}{C_{Total}} \right) \left( \frac{V_{DD}}{2} \right) = \frac{1}{0} \cdot \frac{0.16}{0} \]

\[ N = 8 \]

\[ \left[ 1 + \frac{7}{64} \right] \left( 0.4 \right) = 1 \cdot 0.16 \leq 0.3 \]

(70% power saving)

Parallel Processing

\[ P_{Parallel} = \left( 1 + \frac{C_{Total}}{C_{Total}} \right) \frac{V_{DD}^2}{2} f_{clock} \]

Reduction of Switched Capacitance

\[ \frac{P_{Parallel}}{P_{Total}} = \left( 1 + \frac{C_{Total}}{C_{Total}} \right) \frac{V_{DD}^2}{2} f_{clock} \]

\[ \frac{P_{Parallel}}{P_{Total}} = \left( 1 + \frac{C_{Total}}{C_{Total}} \right) \frac{V_{DD}^2}{2} f_{clock} \]
Glitch Reduction

\[ E = \overline{AB} \overline{C} + \overline{AB} + \overline{C} \]

Glitch due to delay of D

\[ (A \oplus B)(C \oplus B) = F \]

Glitch prone

less glitch-prone

Faster Clocking

Example: N-bit number comparator

Geneva clock

Energy stored in the capacitor

\[ E_{cap} = \frac{1}{2} CV_{c}^{2} \]  

(1)

Energy dissipated in R is

\[ E_{dissip} = \frac{RC}{t} C V_{c}^{2} \]  

(2)

For \( t \gg RC \), \( E_{dissip} < E_{c} \)

why the constant current source is used to “slowly” charge the capacitor, dissipating energy can be made smaller \( \left( < E_{c} \right) \). If the source current direction is reversed, then the energy stored in the capacitor \( E_{cap} \) can be returned! The slower the time, the more can be returned.

Adiabatic Circuits

\[ \begin{align*}
\frac{dV_{c}}{dt} &= \frac{1}{t} \frac{dV_{source}}{dt} \quad \text{Source} = \frac{1}{R} C V_{c}^{2} \\
E_{dissip}(t) &= R C V_{c}^{2} t \\
E_{dissip}(t) &= C V_{c}^{2} \quad \text{t=0} \\
E_{dissip}(t) &= C V_{c}^{2} \quad \text{t=T} \\
\end{align*} \]  

(3)

(4)

Circuit Example

When X is high

\[ V_{in} = 1 \]

\[ V_{out} = 0 \]

\[ E_{dissip} = \frac{1}{2} CV_{source}^{2} \]

\[ E_{dissip} < E_{c} \]
Example
\[ \frac{V}{I} = \frac{3.8\,V}{4.6\,mA} = 0.83 \Omega \]
\[ R_L = 1.5 \Omega \]
\[ \text{For } \frac{V}{I} = 10, \]
\[ \Rightarrow \frac{3.8}{I} = 10 \]
\[ I = 0.38 \, mA \]
\[ V = 1.5 \times 0.38 = 0.57 \, V \]
\[ I_R = 0.38 \, mA \]
\[ R_T = 5.4 \, k\Omega \]
\[ R_F = 1.5 \, k\Omega \]
\[ R_{EF} = R_T \times R_F = 5.4 \times 1.5 = 8.1 \, k\Omega \]
\[ T = \frac{1}{22} \times 10^{-3} = 0.91 \times 10^{-3} \, \text{s} \]

![Diagrams and equations related to electrical circuits and analysis.](image-url)
A More Generalized Analysis of Adiabatic Circuits

\[ E_R(\phi) = \frac{1}{\omega RC} \frac{\omega R C \phi}{1 + \omega R C \phi} \frac{\omega R C}{R} \]
\[ E_C(\phi) = \frac{1}{C} \frac{V_{out}(\phi)}{V_{out}(\phi)} \frac{1}{K} \frac{V_{out}(\phi)}{V_{out}(\phi)} \]

\[ E_R(\phi) = \frac{V_{in}(\phi)}{R} \]
\[ E_C(\phi) = \frac{1}{C} \frac{V_{out}(\phi)}{V_{out}(\phi)} \frac{1}{K} \frac{V_{out}(\phi)}{V_{out}(\phi)} \]

\[ \alpha = \frac{1}{\omega RC} \text{ is high when } \omega RC \text{ is small} \]

\[ \alpha = \frac{1}{\omega RC} \text{ is made small} \]

Adiabatic Clock

\[ \alpha = \frac{1}{\omega RC} \text{ (resonance freq) = } \frac{1}{\omega RC} \]
\[ V_{out}(\phi) = \frac{V_{in}(\phi)}{R} \text{ (power clock)} \]

Energy Efficient Comparator in ADC

\[ V_{in}(\phi) = \frac{3}{8} \frac{V_{out}(\phi)}{2} + \frac{1}{4} \]
\[ V_{in}(\phi) = \frac{3}{8} \frac{V_{out}(\phi)}{2} + \frac{1}{4} \]

Adiabatic charging for 3 bits only since for lower bits savings are < \alpha.
Traditional

Reset switch initializes \( V_{\text{DAC}} \) to \( V_{\text{ref}} \pm \sqrt{\frac{kT}{C_{\text{total}}}} \)

\( C_{\text{total}} = 2 C_{\text{ref}} + C_{\text{CMB}} \), \( T = \text{temperature} \)°C

Alternative Scheme

\[ C_{Q2} = \frac{C_{\text{ref}} (C_{\text{MSP}} - C_{\text{CMB}})}{C_{\text{MSP}} + (C_{\text{ref}} - C_{\text{CMB}})} = C_{\text{MSP}} (1 - \frac{C_{\text{ref}}}{C_{\text{CMB}}}) \]

Swapping energy is reduced by \( x^3 \) (with \( n=3 \))

\( V = 1 \) \( V_{\text{DAC}} = \frac{1}{2} \mu \text{F} \)

\( C_{\text{MSP}} = 100 \mu \text{F} \)

\( C_{Q2} = 1 \mu \text{F} (1 - \frac{1}{500 \mu \text{F}}) = 8 \mu \text{F} \)

\[ V_0 = \frac{1}{2} V \cdot 100 \mu \text{F} + V(0.8 \mu \text{F}) \]

\[ = 200 \mu \text{F} + 0.8 \mu \text{F} \]

\[ = 0.37 \mu \text{V} \]

\( V_{\text{DAC}} = 0.37 \mu \text{V} - \frac{100}{100 + 400} = 0.024 \mu \text{V} \)

\[ V_{\text{DAC}} = 0.37 \mu \text{V} \]