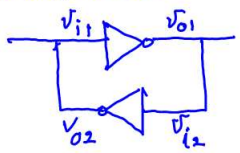
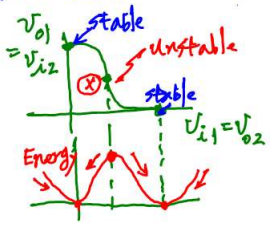
EE 222 Lecture 5C, Jan 22, 2019

Bistable Latch





Two stable points

$(v_{i1}=v_{o2}=V_{DD},\ v_{o1}=v_{i2}=0)$

& $(v_{i1}=v_{o2}=0,\ v_{o1}=v_{i2}=V_{DD})$

The Point ⊗ where $v_{i1}(=v_{o2}) = v_{o1}(=v_{i2})$ is unstable

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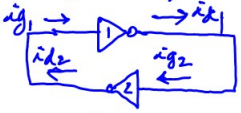
Small signal analysis at ⊗.



$$i_{g1} = i_{d2} = g_m v_{g2}$$
$$i_{g2} = i_{d1} = g_m v_{g1} \quad \text{(1)}$$

$$v_{g1} = \frac{q_1}{C_g} \qquad v_{g2} = \frac{q_2}{C_g} \quad \text{(2)}$$

Also
$$i_{g1} = C_g \frac{dv_{g1}}{dt}$$
$$i_{g2} = C_g \frac{dv_{g2}}{dt} \quad \text{(3)}$$

From (1) & (3)
$$g_m v_{g2} = C_g \frac{dv_{g1}}{dt}$$
$$g_m v_{g1} = C_g \frac{dv_{g2}}{dt} \quad \text{(4)}$$

From (4)

$$g_m v_{g2} = C_g \frac{dv_{g1}}{dt} = C_g \frac{d}{dt}\left(\frac{C_g}{g_m}\frac{dv_{g2}}{dt}\right)$$

$$g_m v_{g2} = \frac{C_g^2}{g_m}\frac{d^2 v_{g2}}{dt^2}$$

$$\frac{d^2 v_{g2}}{dt^2} - \left(\frac{g_m}{C_g}\right)^2 v_{g2} = 0$$

let $\frac{1}{\tau} = \frac{g_m}{C_g}$, then $\frac{d^2 v_{g2}}{dt^2} - \left(\frac{1}{\tau}\right)^2 v_{g2} = 0$

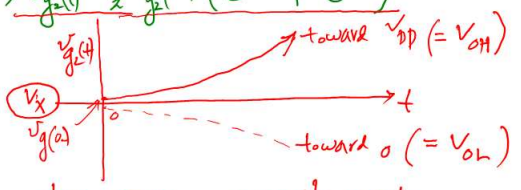
solving for v_{g2} by Laplace transformation

$$s^2 V_{g2}(s) - s v_{g2}(0-) - v_{g2}'(0-) - \left(\frac{1}{\tau}\right)^2 V_{g2}(s) = 0$$

For $v_{g2}(0-) = 0$

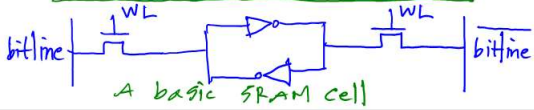
$$V_{g2}(s) = \frac{s v_{g2}(0-)}{s^2 - \left(\frac{1}{\tau}\right)^2} = \frac{1}{2} v_{g2}(0)\left[\frac{1}{s+\frac{1}{\tau}} + \frac{1}{s-\frac{1}{\tau}}\right]$$

$$\Rightarrow v_{g2}(t) = \frac{1}{2} v_{g2}(0-)\left(e^{-t/\tau} + e^{+t/\tau}\right)$$

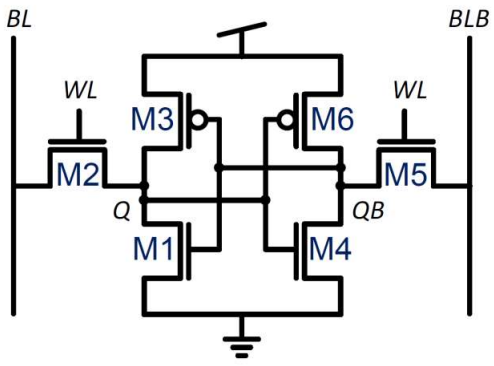


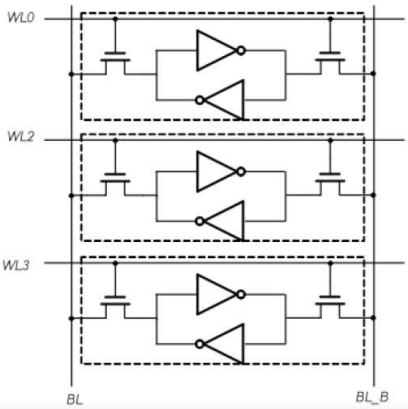
Thus ⊗ is an unstable point

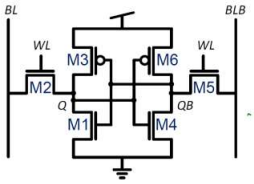
Any perturbation will lead to migration to a stable point (V_{OH} or V_{OL})

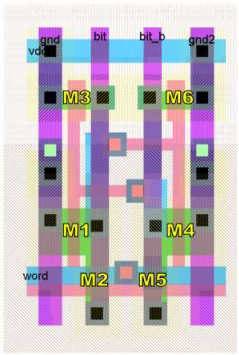


A basic SRAM cell



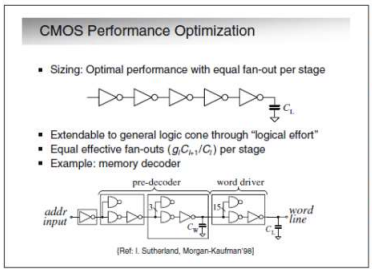






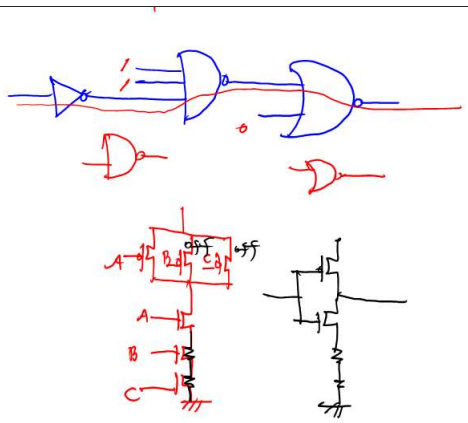
Two sides of the bitcell

- Share Horizontal Routing (WWL).
- Share Vertical Routing (BL, BLB).
- Share Power and Ground.
- Word line routed double on Poly and Metal (reduce resistance)



Slide 3.38
This philosophy is best-reflected in the popular "logical effort"-based design optimization methodology. The delay of a circuit is minimized if the "effective fan-out" of each stage is made equal (and set to a value of approximately 4). Though this technique is very powerful, it also *guarantees* that power consumption is maximal. In the coming chapters, we will reformulate the logical-effort methodology to bring power into the equation.

* Logical Effort : Designing Fast CMOS Circuits
by Ivan Sutherland, David Sproul, David Harris
Morgan Kaufmann Publishers, 1999



Power Minimization

$P = C V_{DD} \Delta V_{swing} f_{clock}$

$\overset{\text{full swing case}}{=} C V_{DD}^2 f_{clock}$

$P = V_{DD} \cdot I$ $\quad I = \frac{C \Delta V}{T} = C \Delta V f_{clock}$

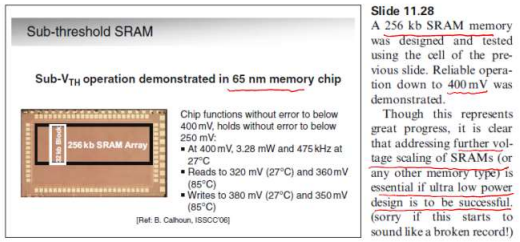
For a given f_{clock},

$\min P = C V_{DD}^2 f_{clock}$
subject to delay < delay specification

$\Rightarrow$ reduce C, V_{DD} (big influence)

delay $\propto \frac{C V_{DD}}{W}$, $C = f(W(\text{tr. size}), \text{interconnect})$

Increasing W reduces delay, but increase C, thus P



Slide 11.28
A 256 kb SRAM memory was designed and tested using the cell of the previous slide. Reliable operation down to 400 mV was demonstrated.
Though this represents great progress, it is clear that addressing further voltage scaling of SRAMs (or any other memory type) is essential if ultra low power design is to be successful. (sorry if this starts to sound like a broken record!)