EE 222 Lecture 5, Jan 22, 2019

Bistable latch

\[ v_{i1}, v_{o1} \]

\[ v_{i2}, v_{o2} \]

Two stable points

\[ (v_{i1} = v_{o1} = v_{dd}, v_{i2} = v_{ss} = 0) \]

\[ (v_{i1} = v_{o2} = 0, v_{i2} = v_{ss} = v_{dd}) \]

The point where \( v_{i1} = v_{i2} \) is unstable.

Small signal analysis at \( \times \).

\[
\begin{align*}
    \frac{\partial^2 V_{g1}}{\partial t^2} + \frac{\partial V_{g1}}{\partial t} &= 0 \\
    \frac{\partial^2 V_{g2}}{\partial t^2} + \frac{\partial V_{g2}}{\partial t} &= 0
\end{align*}
\]

From (1) and (2),

\[
\begin{align*}
    \frac{\partial V_{g1}}{\partial t} &= \frac{g_m V_{g2}}{2} \\
    \frac{\partial V_{g2}}{\partial t} &= \frac{g_m V_{g1}}{2}
\end{align*}
\]

From (1) and (2),

\[
\begin{align*}
    g_m V_{g2} &= \frac{g_m V_{g1}}{2} \\
    g_m V_{g1} &= \frac{g_m V_{g2}}{2}
\end{align*}
\]

Thus \( \times \) is an unstable point.

Any perturbation will lead to migration to a stable point (VDDL or VDDH).

\[ \text{A basic SRAM cell} \]

\[ \text{bitline} \]

\[ \text{bitline} \]
Two sides of the bitcell
- Share Horizontal Routing (WWL).
- Share Vertical Routing (BL, BLB).
- Share Power and Ground.
- Word line routed double on Poly and Metal (reduce resistance)

![CMOS Performance Optimization](image)

**Slide 3.38**

This philosophy is best-reflected in the popular "logical effort"-based design optimization methodology. The delay of a flip-flop is minimized if the "effort input," or the number of stages, is as small as possible. Although this technique is effective, it is important to note that power consumption is high.

While studying CMOS circuits, we will reformulate the logical effort methodology to bring power into the equation.

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**Parity Minimization**

\[ P = C \cdot V_{pp} \cdot V_{out} \cdot \text{Delay} \]

For a given \( V_{out} \),

\[ \min P = C \cdot V_{pp} \cdot \text{Delay} \]

subject to \( \text{Delay} < \text{Delay Spec} \)

\[ \Rightarrow \text{reduce } C \text{, } V_{pp} \text{ (big influence)} \]

\[ \text{delay} < C \cdot V_{pp} \text{, } C = \frac{V_{pp}}{V_{out}} \text{, increasing } \]

increases \( V_{out} \) reduces delay, but increases \( C \), thus \( P \).

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**Slide 11.29**

A 256-kb SRAM memory was designed and tested using the cell of the previous slide. Reliable operation down to 400 mV was demonstrated.

Though this represents great progress, it is clear that addressing further voltage scaling of SRAMs for any other memory type is essential if ultra low power design is to be achievable.

(Notice if this starts to sound like a broken record)...