EE222 Lecture #1 Jan 8, 2019

Instructor Steve Kang (http://nis1.soe.ucsc.edu)

Website https://ee222-winter19-01.courses.soe.ucsc.edu

Webcast https://webcast.ucsc.edu (EE 222)

SmK123

Syllabus – see the website

HWs assigned, but not collected

1st Midterm Feb. 5 (35%)

project proposal due on Feb. 6

2nd Midterm March 7 (35%)

Presentations March 12, 14 (30%)

10% presentation ; 20% written report

Textbook : CMOS Digital Integrated Circuits Analysis & Design, Steve Kang UCSC EE version

Ref 1 : Jan Rabaey, Low Power Design Essentials Springer 2009

Ref 2 : Rahul Sarpeshkar, Ultra Low Power Bioelectronics, Cambridge Univ. Press 2010

Ref 3 : Digest of IEEE Solid-State Circuits Conf. (ISSCC) 2018

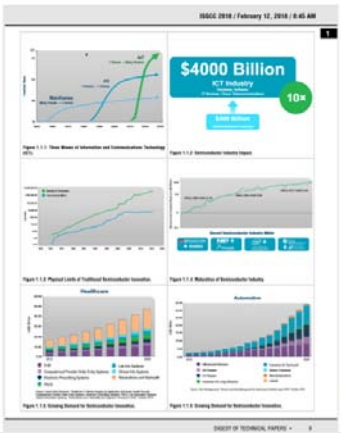
Lecture #1 Textbook chap 1

Ref 1 pp 1-23

Ref 2 pp 1-27

HW #1 Prob. 1.1 (textbook)

Prob. 1.3 (")



Ref 3

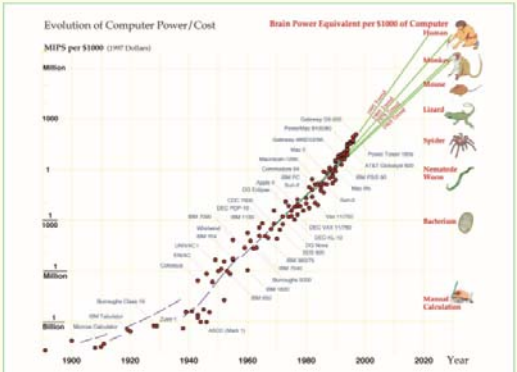
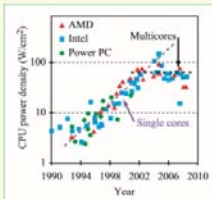
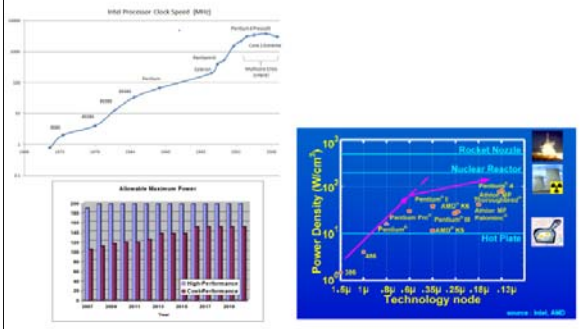


Figure TF1-6: Time plot of computer processing power in MIPS per $1000. (From "When will computer hardware match the human brain?" by Hans Moravec, *Journal of Transhumanism*, Vol. 1, 1998.)



	Light Bulb	Integrated Circuit
Power dissipation	100 W	50 W
Surface area	106 cm² (bulb surface area)	1.5 cm² (die area)
Heat flux	0.9 W/cm²	33.3 W/cm²

Figure TF1-5: (a) Plot of heat power density generated by consumer processors over time, (b) comparison of heat power generation of a light bulb with that of a typical processor.



Source: Intel, AMD

16

Power: The Dominant Design Constraint (1)

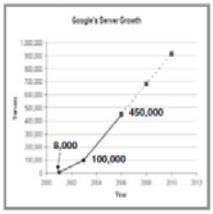
Cost of large data centers solely determined by power bill …

Google Data Center, The Dalles, Oregon

- 400 Millions of Personal Computers worldwide (Year 2000)
  - Assumed to consume 0.16 Tera (10^{12}) kWh per year
  - Equivalent to 26 nuclear power plants
- Over 1 Giga kWh per year just for cooling
  - Including manufacturing electricity

[Ref: Bar-Cohen et al., 2000]

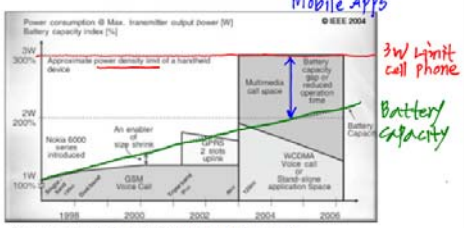
NY Times, June 06



(Ref. 1)

Power : The Dominant Design Constraint (2)

Mobile Apps



3W Limit cell phone

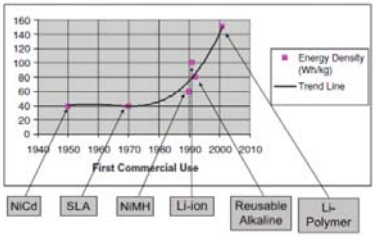
Battery capacity

Power consumption and battery capacity trends

[Ref: Y. Nuevo, ISSCC'04]

(Ref. 1)

Battery Evolution



Accelerated since the 1990s, but slower than IC power growth.

(Ref. 1)

Current Battery Technology is Inadequate

Battery	Rechargeable?	Wh/lb	Wh/litre
Alkaline MnO2	NO	65.8	347
Silver Oxide	NO	60	500
Li/MnO2	NO	105	550
Zinc Air	NO	140	1150
NiCd	YES	23	125
Li-Polymer	YES	65-90	300-415

- Example: 20-watt battery
  - NiCd weighs 0.5 kg, lasts 1 hr, and costs $20
  - Comparable Li-Ion lasts 3 hrs, but costs > 4x more

3

Integrated System Design

Power: The Dominant Design Constraint (3)

Exciting emerging applications requiring "zero-power"

Example: Computation/communication nodes for wireless sensor networks

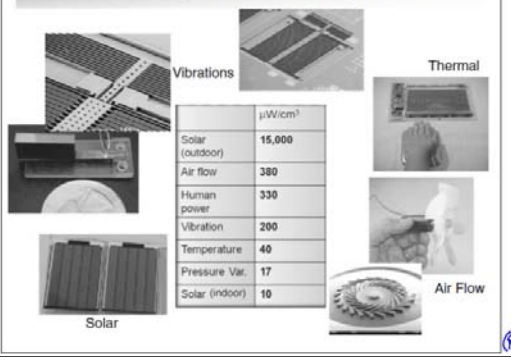
Meso-scale low-cost wireless transceivers for ubiquitous wireless data acquisition that

- are fully integrated
  - size smaller than 1 cm³
- are dirt cheap
  - at or below 1$
- minimize power/energy dissipation
  - limiting power dissipation to 100 µW enables energy scavenging, and
- form self-configuring, robust, ad hoc networks containing 100s to 1000s of nodes

[Ref: J. Rabaey, ISSCC'01]

(Ref. 1)

How Much Energy Can One Scavenge in 1 cm³?



	μW/cm³
Solar (outdoor)	15,000
Air flow	380
Human power	330
Vibration	200
Temperature	40
Pressure Var.	17
Solar (indoor)	10

(Ref. 1)

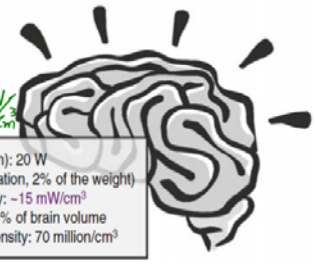
Bio-inspired, neuromorphic computing

A Side Note: What Can One Do with 1 cm³?

Reference case: the human brain

Average brain size $1.33\,(dm)^3$

$\frac{20W}{1.33\times10^3 cm^3} \approx 15\,mW/cm^3$



P_{avg}(brain): 20 W
(20% of the total dissipation, 2% of the weight)
Power density: ~15 mW/cm³
Nerve cells only 4% of brain volume
Average neuron density: 70 million/cm³

(Ref. 1)

Power Dissipation for Load Capacitance C, Power Supply V_{DD}, operating freq f, voltage swing ΔV

$$P = C V_{DD} \Delta V f$$

Scaling factor $k > 1$

- constant-voltage scaling:

$$P_{scaled} = (kC)\, V_{DD} \Delta V\, k^2 f = k^3 (C V_{DD} \Delta V f)$$

- with voltage scaling

$$\hat{P}_{scale} = kC \frac{V_{DD}}{k} \frac{\Delta V}{k} k^{1.7} f = k^{0.7} (C V_{DD} \Delta V f)$$

Power in CMOS gates

$$P_{total} = \underbrace{\alpha \cdot C \cdot V^2 \cdot f_{clk}}_{\text{Dynamic}} + \underbrace{Vdd \cdot I_{short-circuit}}_{\text{Short-circuit}} + \underbrace{Vdd \cdot I_{leakage}}_{\text{Leakage}}$$

- Power is governed by the 3 part equation above
  - Dynamic CV^2F (switching) power
    - ~~Currently the largest part, but~~ can make it smaller by lowering Vdd and Vth
  - Leakage Power
    - Subthreshold conduction – gets larger when Vth is lowered
    - Reverse leakage of diodes
  - Short-circuit (crowbar) current
    - Both pull-up and pull-down devices are partially conducting for a small, but finite amount of time
    - Small (<10%) in a well designed circuit, acts like dynamic power (happens only on a transition) so we won't worry about it here

Integrated System Design

Reduce the active load:
- Minimize the circuits
- Use more efficient design
- Charge recycling
- More efficient layout

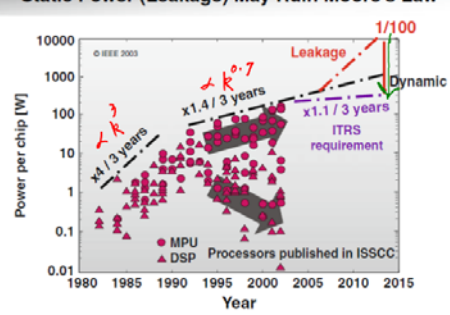
Technology scaling:
- The highest win
- Thresholds should scale
- Leakage starts to byte
- Dynamic voltage scaling

$$P_{sw} = k\, C_L\, V^2_{cc}\, f_{CLK}$$

Reduce Switching Activity:
- Conditional clock
- Conditional precharge
- Switching-off inactive blocks
- Conditional execution

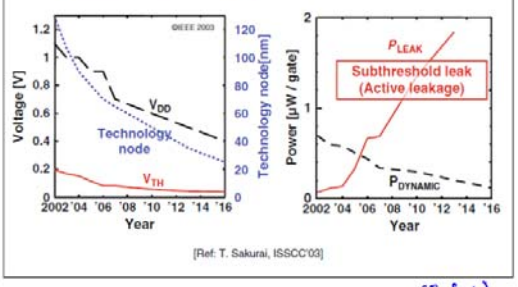
Run it slower:
- Use parallelism
- Less pipeline stages
- Use double-edge flip-flop

Static Power (Leakage) May Ruin Moore's Law



[Ref: T. Sakurai, ISSCC'03]

Sub-threshold Leakage as an Extra Complication

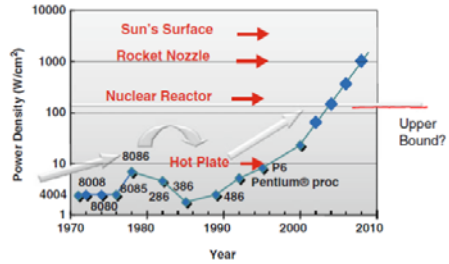


[Ref: T. Sakurai, ISSCC'03]

(Ref. 1)

Power Density Increases

Unsustainable in the long term



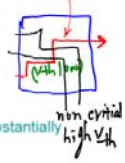
[Courtesy: S. Borkar, Intel]

(Ref. 1)

Barriers to Future Voltage Scaling

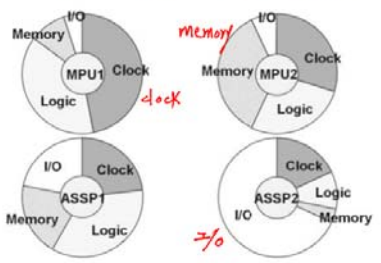
- Voltage scaling requires threshold voltage V_t to be scaled as well (15% per generation)
  - this increases sub-threshold leakage current
  - impact on power consumption and circuit robustness
- Leakage power
  - total leakage current goes up 7.5x per generation
  - leakage power ~~power~~ by 5x
  - ~~soon will become~~ a significant portion of total
    - active power remains constant for constant die size
  - leakage power, and therefore total power, can be substantially reduced by cooling
    - Essential to control die temperature
    - power density (W/cm²): 0.6 micron chips surpassed a hot plate!

critical path



Integrated System Design

Complicating the Issue: The Diversity of SoCs

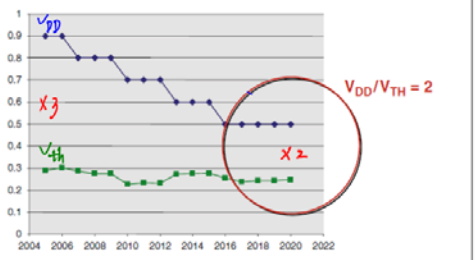


Power budgets of leading general purpose (MPU) and special purpose (ASSP) processors

[Ref: many combined sources]

(R 1)

Supply and Threshold Voltage Trends



Voltage reduction projected to saturate

Optimistic scenario – some claims exist that V_{DD} may get ~~stuck~~ sub 1V area around 1 V

[Ref: ITRS 05, Low power scenario]

(R 1)

An Era of Power-Limited Technology Scaling

Technology innovations offer some relief

- Devices that perform better at low voltage without leaking too much

But also are adding major grief

- Impact of increasing process variations and various failure mechanisms more pronounced in low-power design regime

Most plausible scenario

- Circuit- and system-level solutions essential to keep power/energy dissipation in check
- Slow down growth in computational density and use the obtained slack to control power density increase
- Introduce design techniques to operate circuits at nominal, not worst-case, conditions

(R1)

Metrics for Power

- Power
  - sets battery life in hours
  - problem: power ∝ frequency (slow the system!)
- Energy per operation
  - fixes obvious problem with the power metric
  - but can cheat by doing stuff that will slow the chip
    - Energy/op = Power * Delay/op
- Metric should capture both energy and performance: e.g. Energy/Op * Delay/Op
  - Energy*Delay = Power*(Delay/Op)^2

Figure of Merit (FoM)

Ideally both energy & delay should be low

Integrated System Design

8